

Microcontroller Based Unity Power Factor Converter

by

Mohammed Rafiqul Islam

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

August, 1996

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Mohammed Rafiqul Islam


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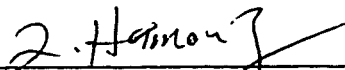
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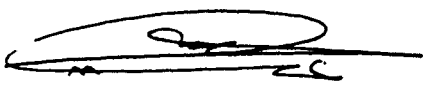

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Dedicated to

My Mother and in the memory of My Father

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Abstract

Name : Mohammed Rafiqul Islam

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To improve power factor and to meet IEC-555-2 harmonic requirements, input power-factor correction circuits are being used widely in the power supply industry. In response to this trend, a microcontroller based pulse-width modulated unity power factor controller has been implemented and tested for a single phase ac to dc converter. Proposed control strategy is suitable for microcontroller based controller and requires minimum hardware. Simulation and experimental results confirm that the supply current can be controlled to keep almost sinusoidal with a near unity power factor by means of the proposed control strategy. Detailed analysis and design equations for the power processing circuit have also been presented.

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تم دراسة وتحليل وتصميم جهاز لتحسين معامل القوى لقالب الجهد المتناوب إلى جهد مستمر أخذين بعين الاعتبار متطلبات المركبات التوافقية (IEC-555-2) . بُني الجهاز باستعمال معالج مكروي متقدم. أثبتت الدراسة النظرية المقترحة مدعماً باستعمال برامج لتمثيلها على الحاسب بأنه يمكن الحصول على معامل قوى مثالي مع المحافظة على شكل جيبي لموجة التيار . ولقد تم التأكد من الدراسة النظرية والتمثيلية بطريقة عملية حيث صمم ونفذ نظام الكتروني بُني على أساس معالج مكروي . أظهرت النتائج النظرية والعملية تقارب كبير جداً . تفاصيل الدراسة والتصميم موضحة خلال فصول البحث .

درجة الماجستير في العلوم

جامعة الملك فهد للبترول والمعادن

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CHAPTER 1

1 INTRODUCTION

Solid-state input power factor conditioners are gradually becoming a must for electronic equipment. Such requirements are particularly relevant to power supplies fed from single phase mains. Applications of these power supplies are in areas such as computers, telecommunications, commercial and domestic appliances (fluorescent lighting, air-conditioning, compressor drives, etc.), battery charging, voltage source inverter, etc.

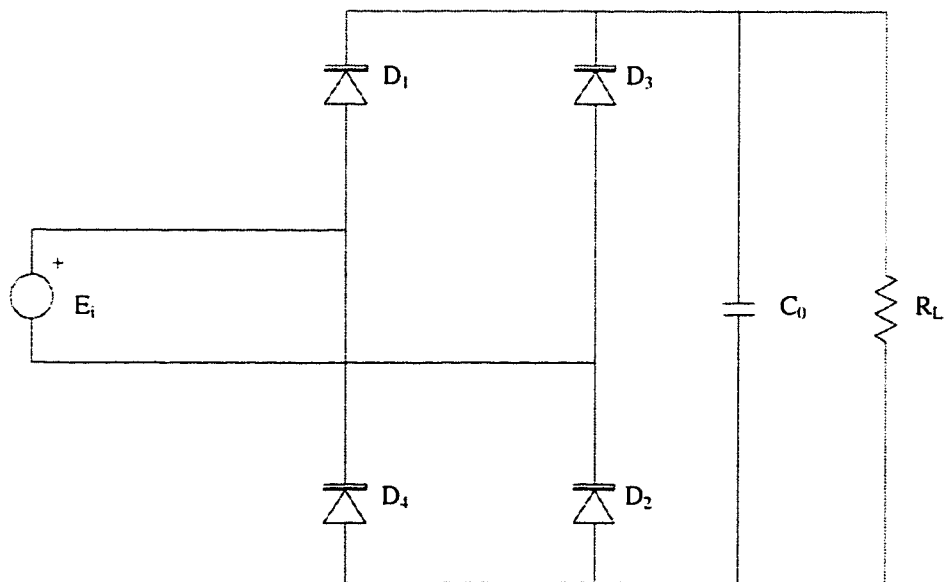


Figure 1.1: Conventional diode rectifier.

The conventional input stage for single phase power supplies (figure 1.1) operates by rectifying the ac line voltage and filtering with large electrolytic capacitor. Such conversion process has several attractive features, such as low cost, compactness, and relatively high operating efficiency, but it has the disadvantage of generating pulsed ac line currents drawn from the ac distribution network. The non-ideal characteristic of these input currents creates a number of problems for the power distribution network and for the other apparatus in the vicinity of the rectifier, and these are as follows:

- They may cause the maloperation of the protective relays,
- Phase displacement of the current and voltage fundamentals require that the source and distribution equipment to handle reactive power, increasing their volt-ampere ratings,
- They cause more losses in power devices due to higher peak current,
- They contain high input current harmonics and low input power factor,
- Rectifier has a lower efficiency because of the large rms values of the input current,
- Input ac mains voltage is distorted,
- Reactive component size is high,
- They may cause insulation breakdown and instrument malfunctions.

Therefore, the reduction of input current harmonics and high power factor operation are important requirements for power supplies, especially when the forthcoming harmonic

standards, such as IEC-555-2, must be satisfied. IEC-555-2 harmonic standards for Class C equipment are shown in table 1.

The Thesis deals with the development and the implementation of Unity Power Factor Converter.

Table 1. IEC-555-2 Harmonic current limits for class C equipment (Lighting)

Harmonic order (n)	Maximum value expressed as a percentage of the fundamental input current
2	2%
3	$30\% \times (\text{power factor})$
5	10%
7	7%
9	5%
$11 \leq n \leq 39$	3%

1.1 Literature Review

Several solutions have been proposed to improve the input power factor and to minimize the harmonics in line current. In general, these techniques can be classified as follows:

- Passive input filter techniques,
- Active filter techniques, and
- Circuits and control techniques

The first two methods concern the suppression of the undesired effects of conventional bridge converter, while the last technique reflects an intent to minimize the harmonics created by the converter and to operate it at improved power factor.

1.1.1 Power Factor Correction by Passive Filter Techniques

A simple way to improve the input current waveform of a conventional diode bridge rectifier is to place an inductor in series with its output (figure 1.2).

This method is easy to implement and relatively cheap. This topology is clearly superior to the conventional diode bridge rectifier. However, the input current contains third harmonic component of considerable amplitude. Therefore, to improve the input power factor a larger filter inductor is required. However, a larger filter inductor has negative impact on the post regulator control strategy. Because larger inductor causes higher ripple in the output dc voltage.

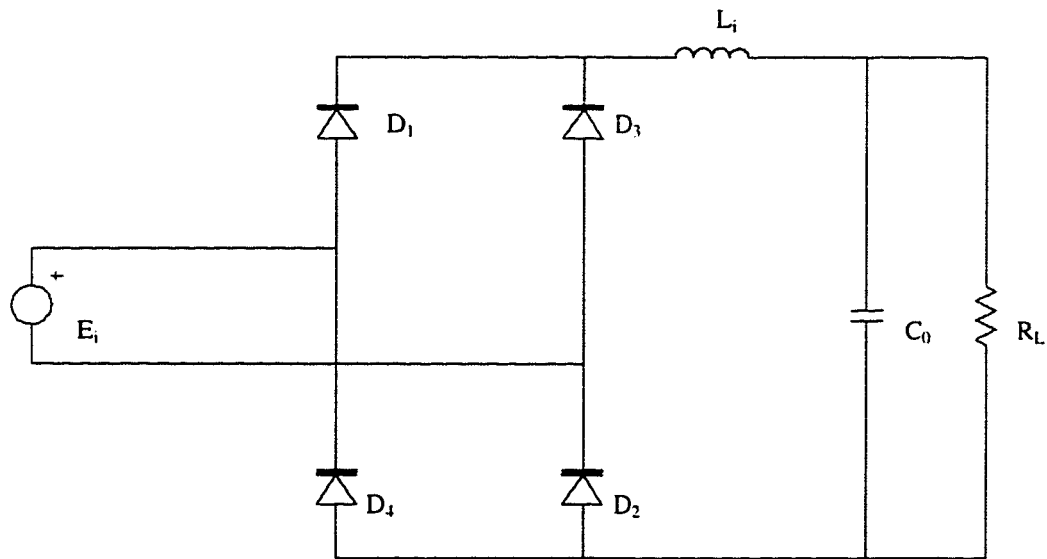


Figure 1.2: Standard diode bridge rectifier.

Input Power factor can be improved by connecting a capacitor C_i (figure 1.3), which has been presented in [1]. But still it has the following disadvantages:

- Low efficiency because of large rms value of the rectifier input current.

- Input ac main's voltage distortion because of the associated rectifier peak currents.

The second disadvantage is particularly important for office or residential applications.

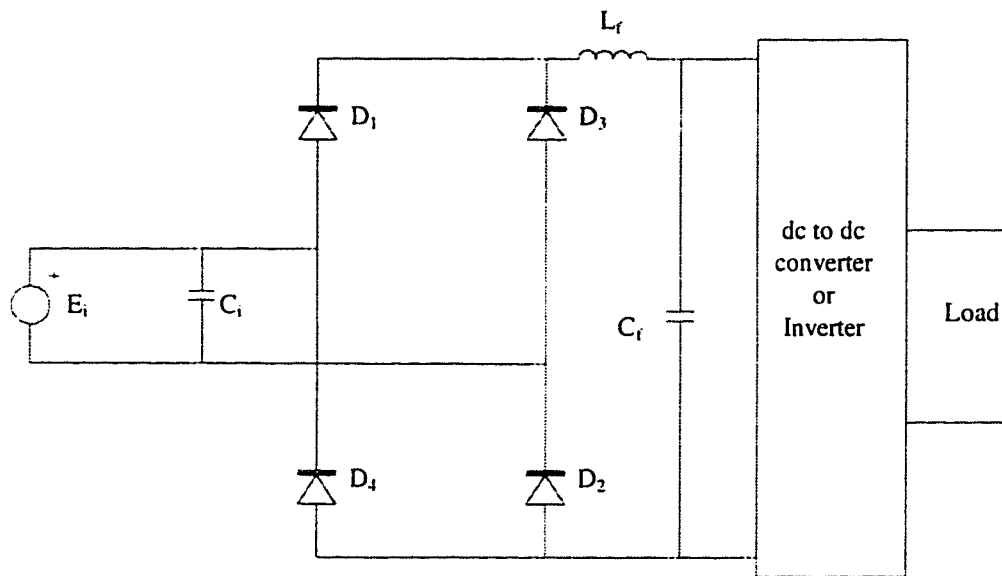


Figure 1.3: Diode rectifier topology with capacitor input filter (Ref. 1).

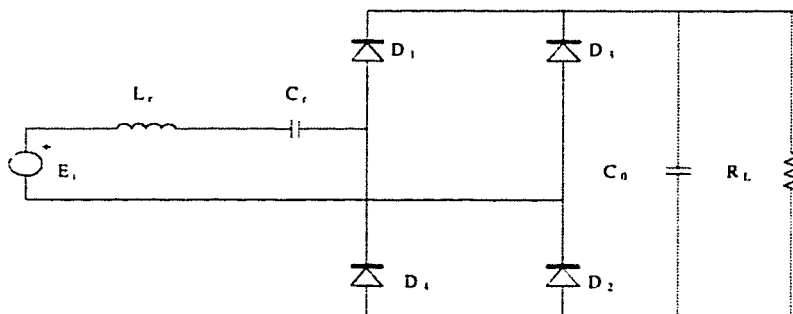


Figure 1.4: Diode rectifier with series resonant filter at input (Ref. 2).

A series resonant filter is another way to passively shape the input current (figure 1.4). A series resonant circuit works as band pass filter. Therefore, if the circuit is tuned at ac line

frequency and if quality factor and characteristic impedance are high enough then the input current will be nearly sinusoidal and power factor will be near unity. The major disadvantages of the series resonant filter is the large size of the reactive elements and large rms current in the capacitors C_0 and C_r .

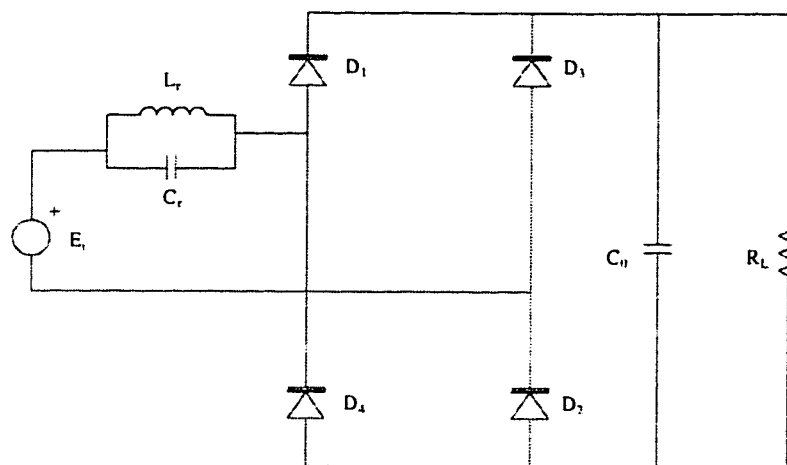


Figure 1.5: Diode rectifier topology with parallel resonant filter (Ref. 2).

If parallel resonant circuit is used, [2] then it is possible to get same performance with lower reactive component size. A rectifier with L-C parallel resonant tank at the input side is shown in figure 1.5. The objective is to make parallel resonance at third harmonic.

The advantages of this configuration over the previously described topology are the followings :

- Lower value of input peak current and hence less input voltage distortion,
- Higher input power factor,
- Increased efficiency because of the low rms values of the input current, and

- Reduced reactive component sizes.

Though the size of reactive components is small compared to the other topologies, it is still high and the power density is low.

1.1.2 Power Factor Correction by Active Filter Techniques

Isao Takahashi proposed a power factor improvement circuit for single phase diode rectifier having high frequency inverter on the load (figure 1.6), [3]. The principle of the improvement is based on dither signal affects for linearization of nonlinear system. Using this principle, a diode rectifier circuit which can be regarded as a dead zone element is linearized by adding a high frequency dither signal to the input voltage. The output voltage of the high frequency inverter is used as dither signal.

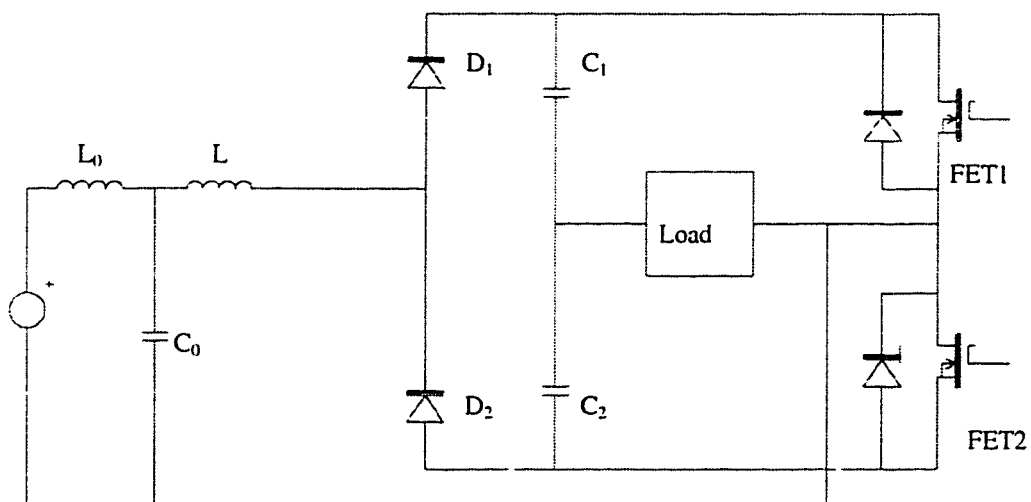


Figure 1.6: Voltage doubler dither rectifier (Ref. 3).

A reduction in reactive component size is achieved. But with the increase of the frequency, commutation loss increases and third harmonic component is 10% of the total current. Although this third harmonic can be canceled by balancing the circuit in three phase systems, most power supplies for low power applications use single phase supply. The inductor, L has to carry the high frequency signal, however, eddy current and hysteresis current losses increase with the increase of frequency. The inductor L needs to be specially designed. For example, it should be composed of ferrite or amorphous core. The maximum dc voltage available is twice the supply voltage amplitude.

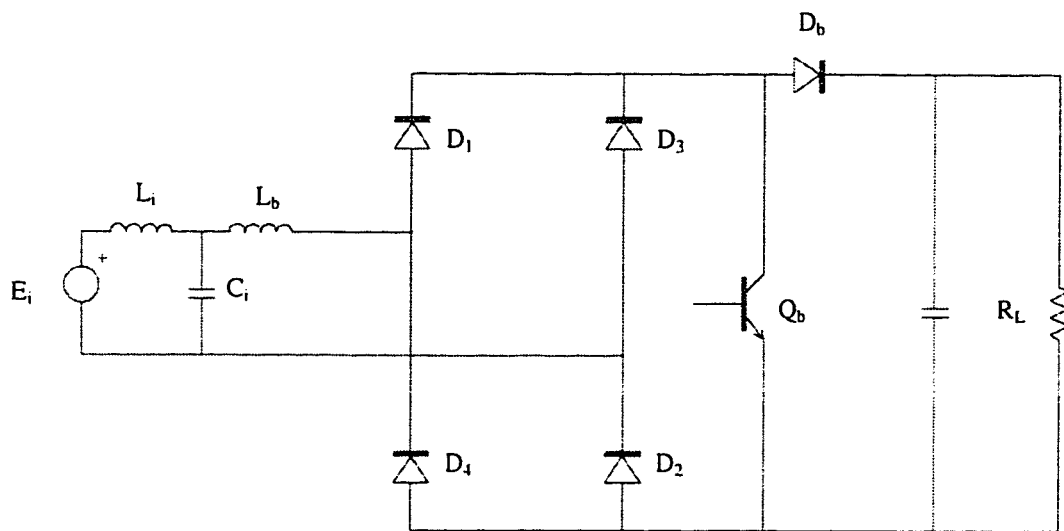


Figure 1.7: Boost rectifier with equal pulse width modulation (Ref. 4).

The boost converter is the most popular topology for off-line non-isolated applications, such as those found in distributed power or modular power supplies. Its major advantage is that the line current is exactly the inductor current, making control relatively simple.

This converter uses boost switch and boost inductor and the boost inductor can be placed in either the dc or ac side.

A single phase boost rectifier, with equal pulse width modulation technique (figure 1.7) to get unity power factor and sinusoidal input current has been presented in [4]. The advantage of the proposed topology is that it gives constant frequency operation. The switching frequency has been selected as multiple of line frequency to avoid the existence of beat frequency in line current. The placement of the inductor in ac side gives reduced ElectroMagnetic Interference (EMI) problem. However, it has the disadvantage of substantially increasing the current stresses of the switching devices so the maximum switching frequency is limited by maximum allowable di/dt of the switching device.

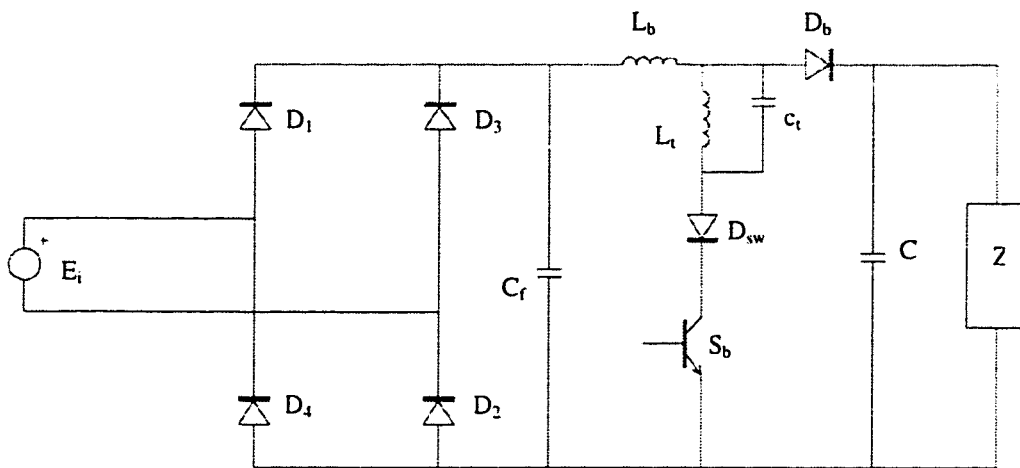


Figure 1.8: Resonant tank boost rectifier (Ref. 5).

L. J. Borle et al. presented a soft switching pulse width modulated ac to dc converter (figure 1.8) that employs a continuously resonating L-C circuit in a single phase single switch boost rectifier circuit in [5].

The resonant technique has the advantage of ensuring on and off of device switch either at zero voltage or at zero current. Thus there will be no voltage and current stress on the device switch and consequently there will be no commutation loss. Since there will be no commutation loss, the size of heat sink of boost switch will be small and in this way we will get higher power density. The resonant technique also reduces the noise and EMI problem. But the disadvantage of this technique is that it requires more reactive components.

1.1.3 Circuits and Control Techniques for Power Factor Correction

Bang-bang hysteresis technique is one of the active current waveshaping technique with the boost converter. A Single phase ac/dc converter that uses bang-bang hysteresis technique has been presented in [6]. In this implementation, instead of diode bridge a diode-capacitor voltage doubler (with inverse parallel power transistor across each diode) has been used (figure 1.9). It can work in rectification as well as in inversion mode. Since regeneration is possible, so the use of this rectifier for driving dc motor results in energy savings for transportation systems with frequent stops.

Though the regeneration is possible, the lower efficiency can not be avoided since the energy stored in the two capacitors is discharged through the supply at the step up process. The capacitor divider configuration is restricted to less than $2\sqrt{2}$ in the voltage step up ratio. Thus wide range operation is not possible. To ensure DC busbar balancing, additional, control loop is required which makes the control scheme complicated. The ripples in output voltage have the following undesirable effects :

- Supply current will contain third harmonic component, which results in distortion.
- Phase of supply current will be shifted which results in reduced power factor.

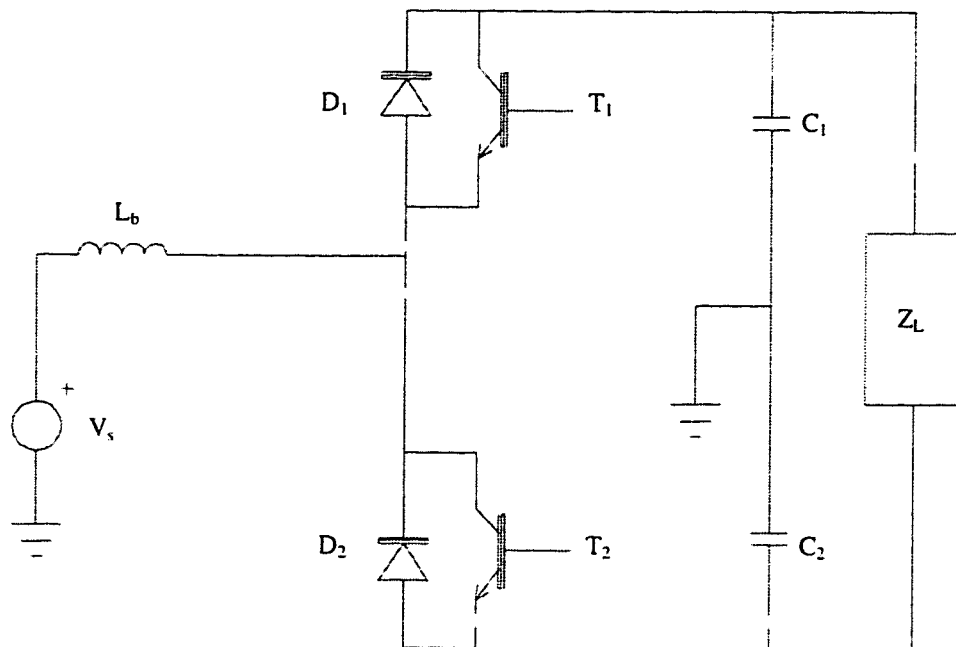


Figure 1.9: Single phase voltage sourced reversible rectifier (Ref. 6).

Therefore, to suppress the third harmonic and to eliminate the phase shift of the supply current, a low pass filter has been introduced in the feed back loop. Since dead time allowance is required between the switching of two transistors, the switching frequency becomes low.

A single phase voltage source ac-dc converter (figure 1.10a) for small power applications, in which regenerative capability is not required has been proposed in [7].

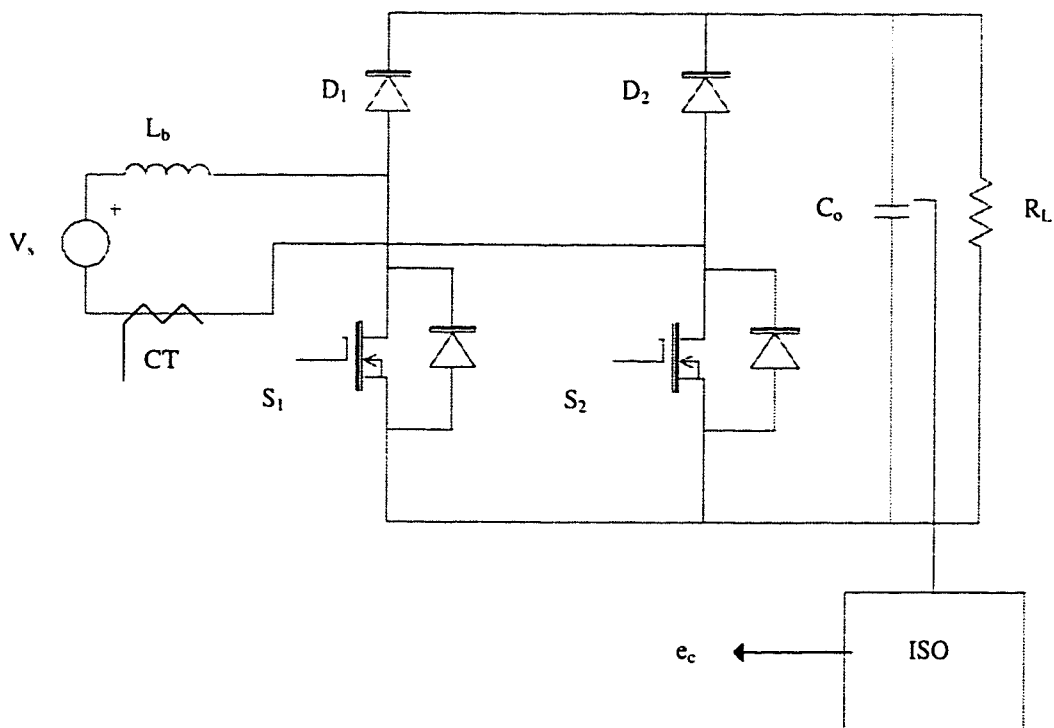


Figure 1.10a: Force commutated single phase ac/dc converter (Ref. 7).

Hysteresis current waveshaping technique has been used to get unity power factor and sinusoidal supply current (figure 1.10b). In this implementation a boost inductor has been placed in ac side. Two MOSFETs are divided into two arms so the dead time allowance to avoid short circuit of the upper and lower devices is not required which is the disadvantage of the topology presented in [6].

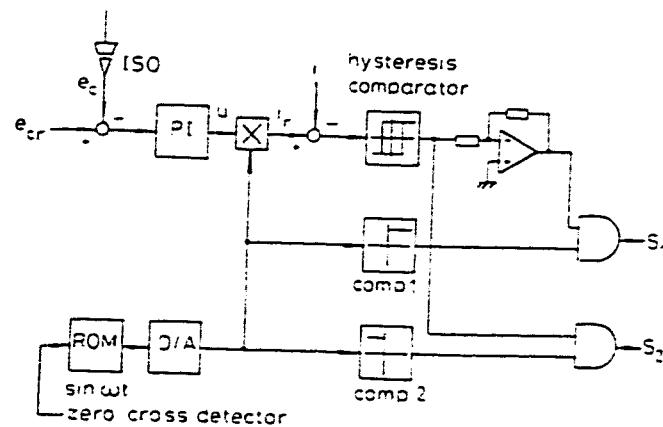


Figure 1.10b: Hysteresis Current control block diagram.

The advantages of this topology are the following:

- The voltage step-up ratio is more than $\sqrt{2}$, so wider operating range is possible,
- Since the sources of both transistors are shorted, only one gate power supply is required,

- Since the diodes conduct in alternate half cycle, simultaneous positive biasing problem of both MOSFET does not occur even if we apply the same gating pulse for both MOSFETs,
- Use of inductor in the ac side will reduce the electromagnetic interference problem, and
- This topology requires less power device and ensures less conduction loss.

Advantage of the Bang- Bang hysteresis technique is that it gives instantaneous current control, which results in very fast response and increased boost switch reliability. However, it has a disadvantage in that the switching frequency of the boost switch is not constant. It depends on load, therefore, the selection of power devices becomes critical, if it is not selected carefully multiswitching problem may arise.

An error triangular current waveshaping technique to get unity power factor and sinusoidal supply current has been proposed in [8]. The schematic diagram of the proposed scheme is shown in figure 1.11. It consists of a diode rectifier and dc/dc converter with front-end solid-state input power factor conditioner. The advantage of this proposed implementation is that it gives nearly sinusoidal current and nearly unity power factor with constant frequency, but the drawback of the proposed implementation is its complexity. The supply current is discontinuous about the zero crossing. It is required to place low pass filter at input side to reduce the EMI. This will increase the size of rectifier and as a result power density will be low.

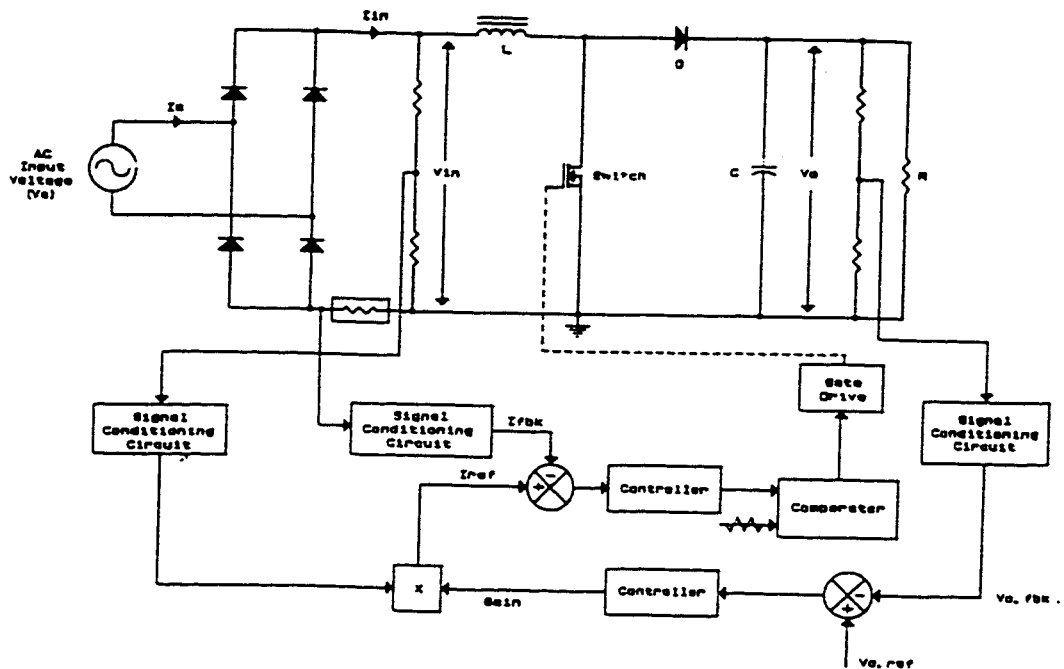


Figure 1.11: Single-phase ac-dc converter with error triangular current waveshaping technique.

G.H.Rim et al. presented a force commuted ac to dc converter (figure 1.12) with analog controller for power factor correction and harmonic elimination of input current [9]. The basic operation of this converter is similar to that proposed in [7], but the current waveshaping technique is different. Instead of hysteresis current control technique, current error triangulation method has been used for waveshaping current waveform. In this topology, instead of feeding directly the step down supply voltage to the multiplier, modified form of the same using non-linear amplifier is fed. This gives the benefit of

eliminating the dead zone of supply current around the zero crossing. Near unity power factor and near sinusoidal supply current with constant switching frequency are reported.

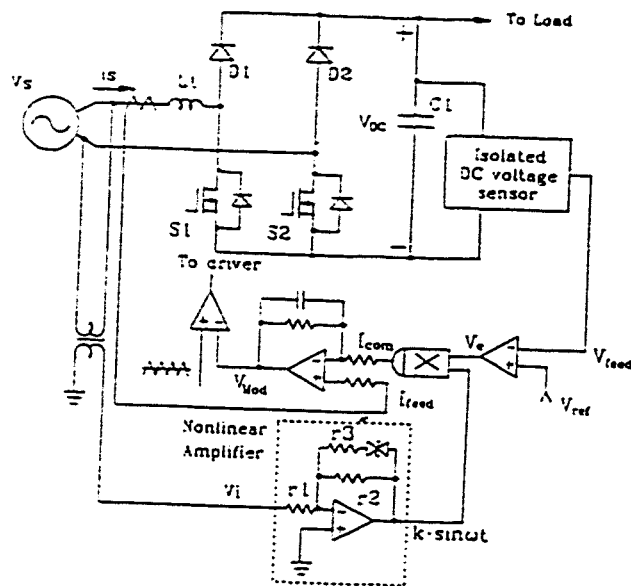


Figure 1.12: Force commuted single-phase ac-dc converter with analog controller for power factor conditioning.

Second-harmonic-injected PWM single phase ac-dc converter with analog controller has been presented in [10]. Constant switching frequency and discontinuous current mode of operation have been used to get the reduction of Total Harmonic Distortion (THD) in supply current. In this scheme only output and input voltages need to be sensed, as a result

monitor circuit is simple. But, because of the discontinuous mode of operation ac low pass filter is must to reject the high frequency component in the supply current.

With switching frequency of 10kHz a THD of 4.3% has been reported with output voltage to input voltage ratio 2.4. Therefore, higher THD is expected with lower ratio of output voltage to input voltage.

A single phase boost converter with analog pulse width prediction controller (PWP) has been presented in [11]. Piecewisely fixed multiple frequency carrier has been used to eliminate the whistling noise in the ac filter that can not be avoided with constant frequency carrier. Carrier frequency of 5, 7, and 9 kHz have been used for $|v_s| \leq 83V$, $83 < |v_s| \leq 128V$ or $|v_s| > 128V$ respectively, where, V_s is the supply voltage. Total Harmonic Distortion of 13% at supply current, 7A has been reported. Therefore, at lower current higher THD is expected.

High frequency power electronic converters are gaining increasing importance these days. Sophisticated control algorithm is required for such converters. Analog techniques [6]-[11] are inadequate for such control scheme. Therefore, digital technique is the only one choice for such converter. Moreover, the control schemes presented in [6]-[11] are implemented by discrete blocks, which does not ensure the compactness.

In the proposed unity power factor converter, the different discrete blocks in the control circuitry have been replaced by a microcontroller without sacrificing the performance.

1.2 Organization of the Thesis

The thesis is organized in the following way: different pulse-width modulation scheme including the proposed one have been described in chapter 2. The circuit topology and operation of the same have been described in chapter 3. The equations for design and component ratings of the power processing circuit have been provided in chapter 4. Microcontroller based control circuitry has been described in chapter 5. Control strategy to get the sinusoidal current and voltage regulation has been described in chapter 6. The simulation and implementation results have been presented in chapter 7. Chapter 8 presents general conclusions and suggestion for future work. The current control algorithm, current control flowchart, and software code have been provided in the appendix.

CHAPTER 2

2 PULSE WIDTH MODULATION

PWM ac to dc converters have many advantages over the phase-controlled ac to dc converter. Firstly, they have no phase shift between line current and the voltage at the input. Secondly, they produce lower harmonic content in the input current. In addition, they produce a better output voltage with less ripple content. Several established PWM techniques are available in the literature, referred as : Equal pulse-width modulation (EPWM), Sinusoidal pulse-width modulation (SPWM), Modified sinusoidal pulse-width modulation (MSPWM), and Delta-modulation also known as Bang-Bang hysteresis technique.

2.1 Equal Pulse Width Modulation Technique

The harmonic content in the input of ac to dc converter can be reduced and hence improved power factor can be achieved by turning 'on' and 'off' the switches of the converter for several times during each half of the input voltage.

The gate signals for the switches are generated by comparing a triangular wave with a dc signal as shown in figure 2.1. With the increase of number of pulses per half cycle lower

order harmonics can be eliminated or reduced. However, increasing the number of pulse would also increase the magnitude of higher order harmonics, which could easily be filtered out.

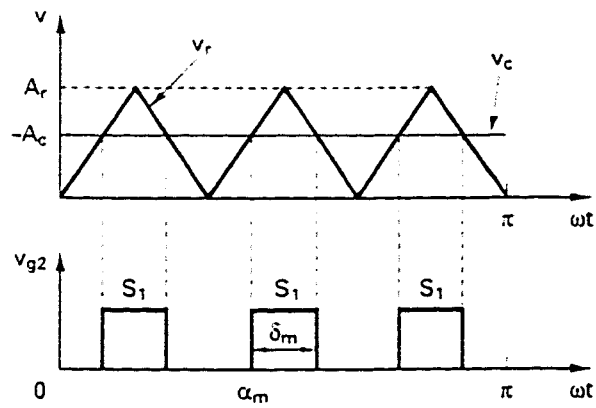


Figure 2.1: Equal pulse-width modulation.

2.2 Sinusoidal Pulse Width Modulation Technique (SPWM)

Instead of maintaining the width of all pulses the same as in the case of equal pulse width modulation, the width of each pulse is varied in proportion to the amplitude of sinwave evaluated at the center of the same pulse.

In sinusoidal pulse width modulation technique as shown in figure 2.2 the pulses are generated by comparing a triangular reference wave V_r of the amplitude A_r and frequency f_r with a carrier half-sinusoidal wave V_c of variable amplitude A_c and frequency $2f_s$. The sinusoidal waveform V_c is in phase with the input voltage V_s and twice the supply

frequency f_c . The widths of the pulses (and the output voltage) are varied by changing the amplitude A_c or the modulation index, M from 0 to 1 which is defined as

$$M = \frac{A_c}{A_r}$$

In this scheme it is possible to get unity displacement factor, and hence improved power factor is achieved . The lower order harmonics are reduced or eliminated.

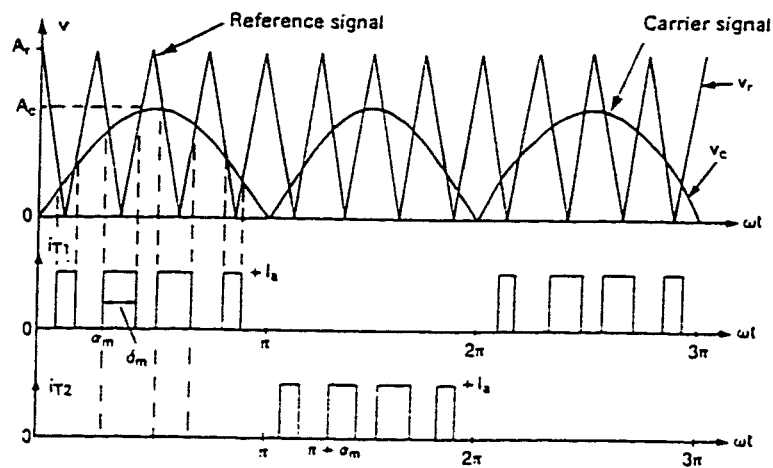


Figure 2.2: Sinusoidal pulse-width modulation.

2.3 Modified Sinusoidal Pulse Width Modulation

In sinusoidal pulse width modulation the widths of pulses that are nearer the peak of the sinewave do not change significantly with the variation of modulation index. This is due to the characteristics of a sinewave, and the SPWM technique can be modified so that the carrier wave is applied during the first and the last 60° intervals per half-cycle. This type of modulation is known as MSPWM and shown in figure 2.3. It gives the reduction in number of switching of power devices and results reduction in switching losses.

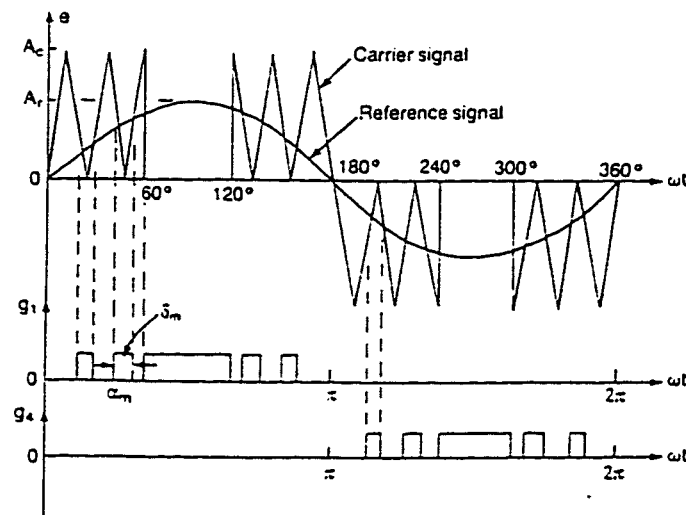


Figure 2.3: Modified sinusoidal pulse-width modulation.

2.4 Delta Modulation

In delta modulation [11] a triangular wave is allowed to oscillate with a defined band, called hysteresis band (Δh) above and below the reference sine wave V_r . The switching pulses for the power devices are generated from the vertices of the triangular wave V_c as shown in figure 2.4.

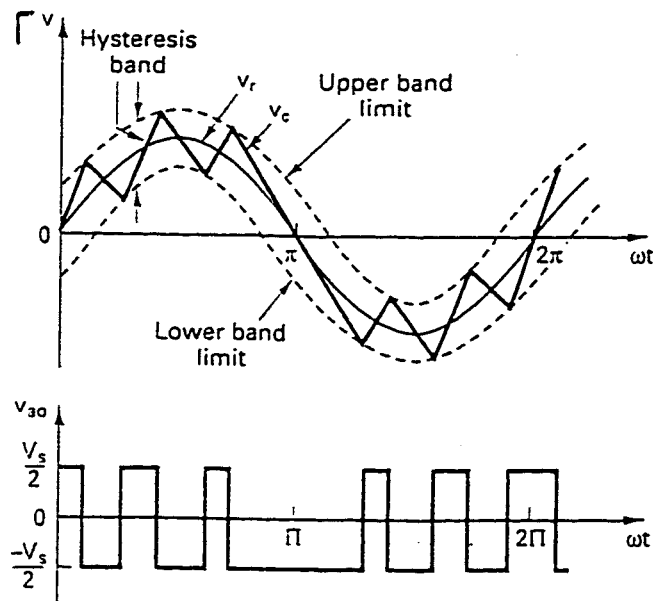


Figure 2.4: Delta modulation.

This scheme is also known as Bang- Bang hysteresis technique. If the frequency of the modulating wave is changed keeping the slope of the triangular wave constant, the number of pulses and pulse widths of the modulated wave would change. This current control technique has been used in [6] and [7]. It gives instantaneous current control that

results in very fast response and increased power switch reliability, but disadvantage of this technique is that switching frequency depends on load, therefore, selection of power devices becomes critical, if it is not selected carefully multischwitching problem may arise.

2.5 The Proposed PWM Strategy

All the PWM strategy discussed before can be used for analog controller since modulating wave need to be sampled continuously for the generation of pulses for power devices. But in digital processor based controller, continuous sampling is not possible. The proposed PWM strategy is the modified version of the delta-modulation to be suited for the microcontroller. The principle of this technique is shown in figure 2.5. Reference wave I_r is the rectified sinusoidal wave. Modulating wave I_c is sampled at regular interval. The reference position for sampling the modulating wave is zero crossing of reference wave. A fixed number of sample is taken for each half of reference wave, let us call it sample group. For the time between the zero crossing and the first sample of a sample group, the gating, pulse is kept at logic '1' state, this eliminates or reduces the dead band. During the regular sampling period, the switching pulses for the power devices are generated from the vertics of the modulating wave. Hysteresis band need not to be defined. If the vertics of the modulating wave exist above the reference wave a pulse of logic '0' is generated, and if the same exists below the reference wave, pulse of logic '1' is generated.

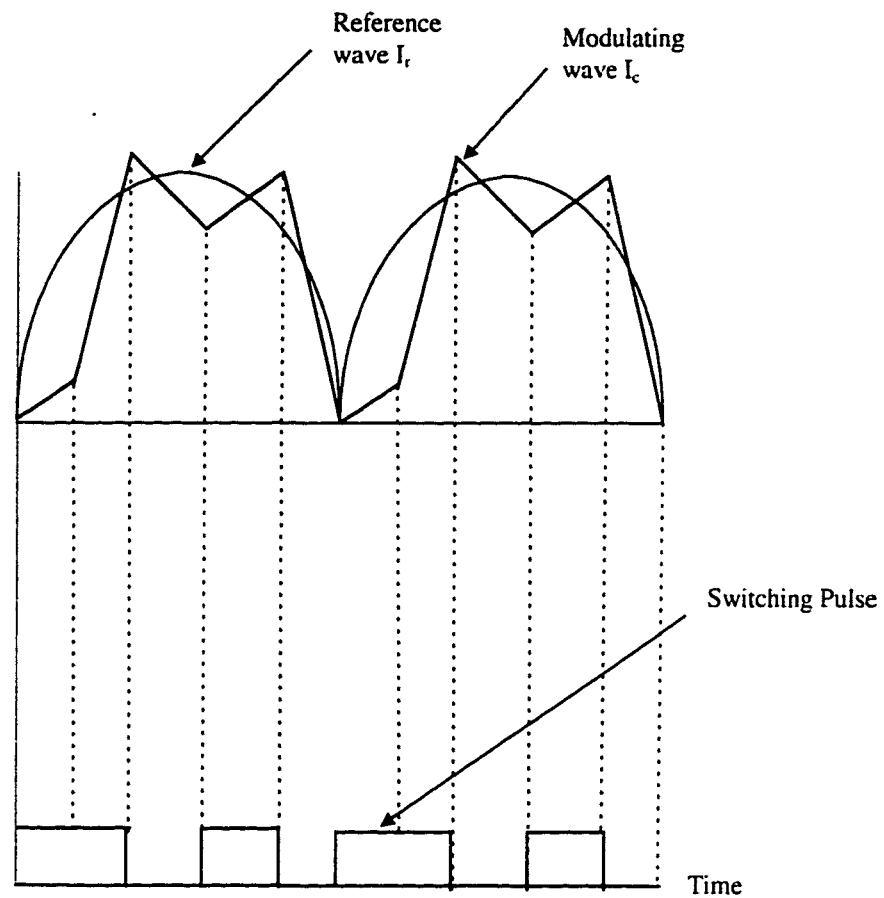


Figure 2.5: Proposed PWM strategy.

In this scheme the upper switching frequency is known in advance, and we can select the power device based on that, therefore, there will be no possibility of multiswitching problem.

CHAPTER 3

3 CIRCUIT TOPOLOGY AND OPERATION

Description of power processing circuit and the operation of the same will be presented in this chapter.

3.1 Circuit Topology

As we have seen from the literature review force commutated ac/dc converter has the advantage over the other topologies. This is because of its lower conduction loss and it requires less power device. Inductor is placed in the ac side of the bridge, it reduces the EMI problem. Therefore, this topology is selected as power processing circuit (figure 3.1) for the proposed unity power factor converter.

The bridge consists of two power diodes, two power MOSFETs. MOSFETs are placed in opposite arms, it has two advantages and they are as follows :

- This configuration eliminates the requirement of dead time allowance, to avoid the short-circuit of the upper and lower devices is not needed with any control scheme that would be required if they were placed in the same arm.

- Source of the two MOSFETs are connected together, therefore only one base drive is sufficient, however, it is sufficient for each MOSFET to obtain the gate signals of a halfcycle and we can eliminate the unnecessary pulses in the other halfcycle using separate base drives for two MOSFETs.

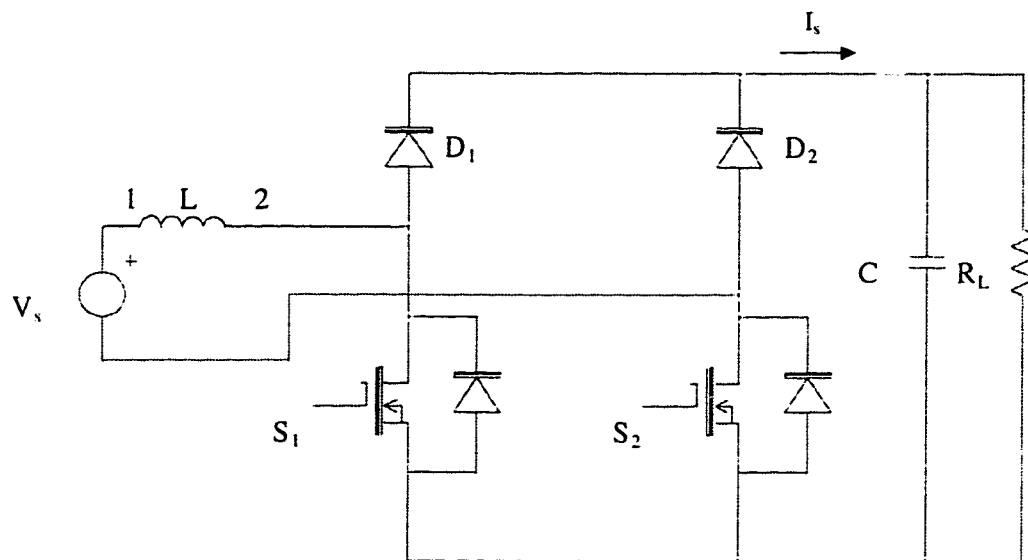


Figure 3.1: Basic circuit topology.

MOSFET is used instead of BJT for two reason:

- MOSFET is a voltage controlled device while BJT is current controlled device. The charge storage problem limits the frequency of operation of BJT.
- MOSFET has integral integral reverse conducting diode, which is available for use, but BJT does not have such feature. If BJT would be used instead of MOSFET then external diodes require to be placed across the emitter and collector of the BJT.

3.2 Circuit Operation

Let us divide the operation of the circuit in four modes, namely, mode 1, mode 2, mode 3 and mode 4. Assuming that the capacitor is pre-charged, the four modes of operations are described as follows :

Mode 1 : When the input voltage is positive if S_1 is turned on, the inductor current (i) increases through S_1 and the body diode of S_2 and magnetic energy is stored in the inductor. Since the diodes D_1 and D_2 are reverse biased, capacitor C supplies power to the load. Neglecting the voltage drop at body diode of S_2 and at MOSFET S_1 equivalent circuit for this mode is shown in figure 3.2.

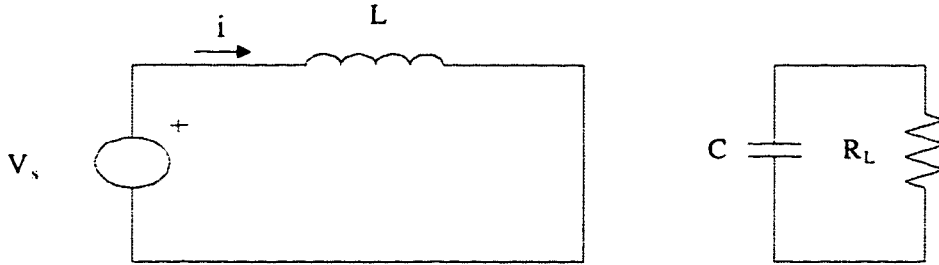


Figure 3.2: Equivalent circuit of the basic circuit at mode 1.

Assuming loss-less inductor, operation of the circuit is given by the equation 3.1 and 3.2 respectively :

$$V_s = L \frac{di}{dt} \quad (3.1)$$

$$\frac{de_c}{dt} = - \frac{e_c}{R_L} \quad (3.2)$$

Where, i and e_c are the inductor current and voltage across the capacitor respectively.

Mode2 : With the input voltage positive, S_1 is turned off, the energy stored in the inductor and the energy from the supply source is transferred through the D_1 and C to the load. The

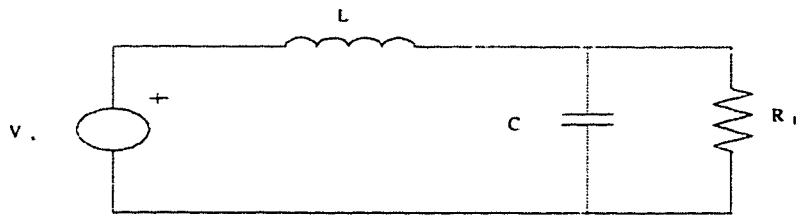


Figure 3.3: Equivalent circuit at mode 2.

return path is through the body diode of S_2 to the supply source. The equivalent circuit in this mode is shown in figure 3.3. Governing equations in this mode are given by 3.3 and 3.4.

$$L\left(\frac{di}{dt}\right) = v - e_c \quad (3.3)$$

$$\frac{de_c}{dt} = \frac{i}{C} - \frac{e_c}{CR_L} \quad (3.4)$$

Mode 3 : When the input voltage is negative, S_2 is turned on, the inductor current is increased through S_2 and the body diode of S_1 and the resultant magnetic energy is stored in the inductor. Again the diodes D_1 and D_2 are reverse biased and C provides the power

to the load. The equivalent circuit for this mode is identical to that of mode 1 and the governing equations are given by equations 3.1 and 3.2.

Mode 4 : With the input voltage negative, S_2 is turned off, the stored energy in the inductor and the energy from the ac source is transferred through D_2 and C and to the load. The return path is through the body diode of S_1 to the supply source.

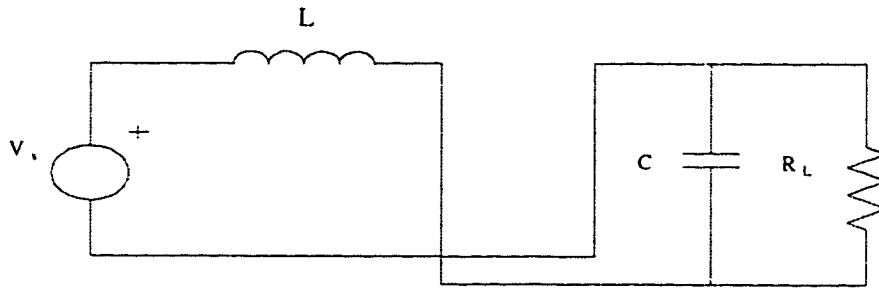


Figure 3.4: Equivalent circuit at mode 4.

The equivalent circuit for this mode is shown in figure 3.4 and the governing equations are given by equations 3.5 and 3.6.

$$L\left(\frac{di}{dt}\right) = v + e_c \quad (3.5)$$

$$\frac{de_c}{dt} = -\frac{i}{C} - \frac{e_c}{CR_L} \quad (3.6)$$

CHAPTER 4

4 CIRCUIT DESIGN

The values of the Inductor and capacitor for the converter circuit are determined and the devices and components' ratings are calculated considering following assumptions :

- a) Converter is lossless,
- b) Load is resistive

Now let us consider that we have the following specifications:

Output power $P_0 = 500 \text{ W}$

Output voltage $V_0 = 220 \text{ V}$

Allowable output voltage ripple $\leq 1.5\%$

Input voltage $V_{in} = 110 \text{ volt}$

Allowable Total Harmonic Distortion(THD) in input current $\leq 5\%$

Displacement factor = 1

Supply frequency $f_1 = 60\text{Hz}$

Switching frequency $f_{sw} = 4.8 \text{ kHz}$

The switching frequency is determined by conversion rate of the A/D converter of the microcontroller, switching losses of the available power MOSFET switches, allowable inductor current ripple, and the quality of reference current tracking. Higher switching

frequency gives lower inductance and hence better transient response and greater power density.

Base values are defined as :

Base Volt-ampere $P_B = P_0 = 500 \text{ VA}$

Base voltage $V_B = V_{in} = 110 \text{ V}$

Base Current $I_B = P_B / V_B = 500/110 = 4.545 \text{ A}$

Base impedance $Z_B = V_B / I_B = 110/4.545 = 24.2 \Omega$

Base frequency $f_B = f_{line} = 60 \text{ Hz}$

Base Inductance $L_B = (Z_B / 2\pi f_B) 10^6 = 64192.5 \mu\text{H}$

Base Capacitance $C_B = (1 / 2\pi f_B Z_B) 10^6 = 109.61 \mu\text{F}$

Now from the power balance between input and output, we get

$I_{in} = 1 \text{ pu}$, $V_0 = 2 \text{ pu}$ and the load resistance $R_L = 4 \text{ pu}$ (96.8Ω)

Inductance and capacitance size will be determined by the allowable THD in input current and ripple in output voltage respectively.

4.1 Design of Boost Inductor, L

Inductor is designed based on the possible maximum switching frequency, for our case it is 4.8 KHz. The inductor current is controlled by the voltage across the inductor. Mode 3 and Mode 4 at $V_{in} \leq 0$ correspond to Mode 1 and Mode 2 at $V_{in} \geq 0$. Now the potential at terminal 1 of inductor (figure 3.1) is supply voltage V_{in} and the same at terminal 2 is

either zero or V_0 depending on the mode of switches S_1 and S_2 . The voltage that contributes to the ripple in input current is the voltage at terminal 2 of inductor. In other words, it can be said that the ripple current is produced by an equivalent square wave of amplitude $V_0/2$ and frequency equal to switching frequency. For 50% duty cycle of switch, error current will track the reference error current, so ripple will be maximum. To consider the worst case for ripple, the duty cycle of the switch is taken to be 50%.

Switched voltage (v_r) that causes ripple in input current can be derived from Fourier analysis of square wave voltage with amplitude $V_0/2$ given by the following equation:

$$v_r = \sum_{n=1,3,5,\dots}^{\infty} \frac{2V_0}{n\pi} \sin(2\pi n f_{sw} t) \quad (4.1)$$

Let V_{1r} and I_{1r} are the RMS values of the fundamental component of the switched voltage and ripple current at switching frequency respectively, so V_{1r} and I_{1r} are related by the following equation:

$$V_{1r} = (2\pi f_{sw} L) I_{1r} \quad (4.2)$$

Assuming ripple in inductor current is due to fundamental (switching frequency) component of ripple current, $I_{1r} = 0.05 I_{in}$.

Putting the value of I_{1r} in terms of I_{in} in equation 4.2 we get

$$L = 1.43 V_0 / f_{sw} I$$

With the values chosen before L is found to be 14.45 mH (0.225 pu).

4.2 Design of Output Filter, C

A high switching frequency does not improve the voltage loop transient response, output filter capacitor is responsible for that and we have to design the C according to specified ripple voltage. To find the value of C for a desired output voltage ripple, we note that the capacitor- resistor combination at the output of the converter acts as a low- pass filter for the current I_s (figure 3.1). The waveform of current I_s for 15 samples/group is shown in figure 4.1.

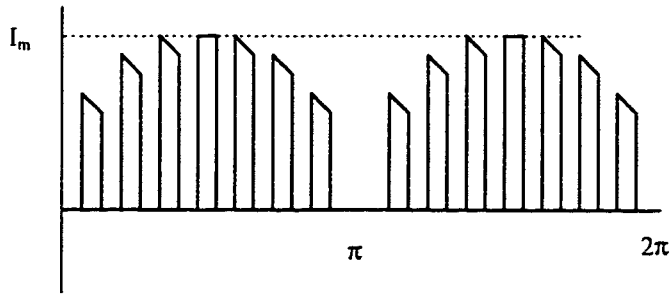


Figure 4.1: Current waveform (I_s) for output capacitor and load resistor combination.

Fourier analysis of this current shows that this current is of a sinusoidal nature, considering only its dc and fundamental components. Therefore,

$$I_s \cong k(1 - \cos 4\pi f_{line} t)$$

where, $k = \frac{I_m}{\pi}$ and I_m is the peak supply current

DC voltage across the load

$$V_{dc} = kR_L$$

Now RMS value of the ripple voltage V_1 is given by the following equation

$$V_1 = \frac{kR_L / \sqrt{2}}{((4\pi f_{line} R_L C)^2 + 1)^{1/2}} \quad (4.3)$$

Therefore,

$$r = \frac{V_1}{V_{dc}} = \frac{1 / \sqrt{2}}{((4\pi f_{line} R_L C)^2 + 1)^{1/2}} \quad (4.4)$$

where, r is the ripple factor

As a result, C can be found in terms of r to be

$$C = \frac{(1 - 2r^2)^{1/2}}{4\sqrt{2}\pi r R_L f_{line}} \quad (4.5)$$

To get the ripple factor of less than 1.5% a capacitor with $C = 645.74 \mu\text{F}$ (17.68 pu) would be adequate.

4.3 Device and Component Ratings

The voltage and current ratings of the device and components of the converter are as follows :

Boost Inductor, L

RMS current : $I_{L,rms} = 4.55 \text{ A}$

Peak current : $I_{L, peak} = I_m = 6.44 \text{ A}$

Capacitor :

RMS ripple Voltage = $V_1 = r * V_{dc} = 1.5 * 220 / 100 = 3.3 \text{ V}$

$$\text{Peak voltage} = 220 + 3.3\sqrt{2} = 224.65 \text{ V}$$

$$120 \text{ Hz ripple current (peak), } I_{r,\text{peak}} = \frac{I_m}{\pi} \frac{R_L}{\sqrt{R_L^2 + X_c^2}} = 2.05 \text{ A}$$

Body diode :

$$\text{Average Current : } I_{B,0} = I_m/\pi = 2.05 \text{ A}$$

$$\text{RMS Current : } I_{B,\text{rms}} = I_m/2 = 3.22 \text{ A}$$

$$\text{Peak current : } I_{B,\text{peak}} = 6.44 \text{ A}$$

MOSFETs :

$$\text{Average drain current: } I_{ds,0} = I_m/2\pi + I_m/\pi = 1.025 + 2.05 = 3.075 \text{ A}$$

$$\text{RMS drain current : } I_{ds,\text{rms}} = \sqrt{\{(I_m/2)^2 + (I_m/2\sqrt{2})^2\}} = 3.95 \text{ A}$$

$$\text{Maximum drain to Source voltage, } V_{ds,\text{max}} = 224.65 \text{ V}$$

Diodes :

$$\text{Average Diode Current : } I_{d,0} = I_m/2\pi = 2.05 \text{ A}$$

$$\text{RMS Diode current : } I_{d,\text{rms}} = I_m/2\sqrt{2} = 2.28 \text{ A}$$

$$\text{Peak current : } I_{d,\text{peak}} = I_m = 6.44 \text{ A}$$

$$\text{Peak Inverse voltage, PIV} = 224.65 \text{ V}$$

4.4 Snubber Circuit Design

Each semiconductor device has finite rate of change of volt. To avoid the damage of the device it is required to keep the $(\frac{dv}{dt})$ to allowable limit. An RC snubber circuit can ensure that. In designing snubber circuit we have to be careful so that the circuit $(\frac{dv}{dt})$ does not exceed the device $(\frac{dv}{dt})$. The snubber circuit should be designed considering $(\frac{dv}{dt})$ which is less than the device $(\frac{dv}{dt})$.

4.4.1 Snubber Circuit for MOSFET

MOSFET with snubber circuit is shown in figure 4.2. $(\frac{dv}{dt})$ of MOSFET is given by

$$(\frac{dv}{dt}) = \frac{V_s}{t_f} \quad (4.6)$$

V_s is the drain to source voltage when it is off, and t_f is the fall time, for our case V_s is the

dc bus voltage V_0 . Circuit $\frac{dv}{dt}$ is given by

$$(\frac{dv}{dt}) = \frac{I_m}{C_s} \quad (4.7)$$

I_m is the peak value of the inductor current.

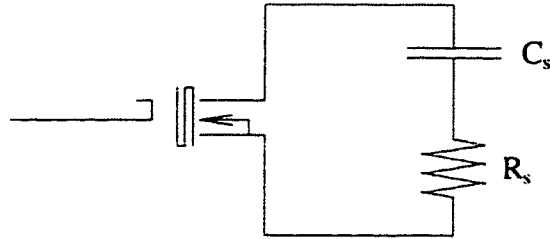


Figure 4.2: MOSFET with RC snubber.

Equating 4.6 and 4.7 we get

$$\frac{V_s}{t_f} = \frac{I_m}{C_s} \quad (4.8)$$

Solving the above equation gives

$$C_s = \frac{I_m t_f}{V_s} \quad (4.9)$$

For IRFP450 $t_f = 60\text{nsec}$, therefore value of C_s comes 1.75 nF

The capacitor is charged during off period of MOSFET, and it is discharged across the MOSFET while the transistor is on. Therefore to limit the discharge current we need to put resistance (R_s) in series to the snubber capacitor (C_s) and the value of R_s is given by following equation :

$$R_s = \frac{V_s}{I_{TD}} \quad (4.10)$$

where I_{TD} is the discharge current, now if we limit the discharge current, to the 10% of the maximum inductor current, then the value of R_s becomes 342.27 Ω .

Power rating of the snubber resistance is given by

$$P_s = 0.5C_s V_s^2 f_s \quad (4.11)$$

where f_s is the switching frequency

For our case maximum possible switching is 4.8 KHz, therefore the power rating of the snubber resistance becomes 203 mW.

4.4.2 Snubber Circuit for Diode

Diode with snubber circuit is shown in figure 4.3. For diode, design equation for finding out the R_s and C_s are given by the following equations :

$$\left(\frac{dv}{dt} \right)_{ckt} = \left(\frac{dv}{dt} \right)_{device} = \frac{0.632 V_s}{C_s R_s} \quad (4.12)$$

$$R_s = \frac{V_s}{I_{TD}} \quad (4.13)$$

From the switching characteristics of the diode being used in our experiment (BYT12P)

we get $\frac{dv}{dt} = 500 \text{ V}/\mu\text{sec}$. Therefore, the value of snubber capacitor C_s and the snubber

resistance (discharge current is limited to 10% of the peak inductor current) become

812.46 pF and 342.27 Ω . The power rating of the resistance is 95 mW.

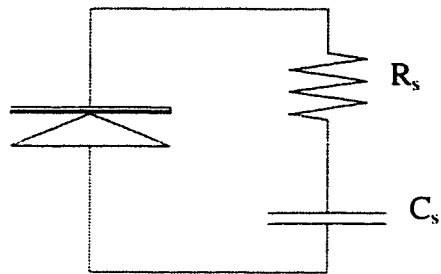


Figure 4.3: Diode with snubber.

CHAPTER 5

5 CONTROL CIRCUITRY AND INTERFACING

Power factor correction circuit consists of two major functional blocks: Power processing and control. The operation of the power processing circuit has been described in chapter 3. In this chapter the operations of the control block and interfacing circuit have been presented.

5.1 Control Circuitry

The control block of the proposed unity power factor converter is shown in figure 5.1. It consists of a microcontroller (68HC11) with E-Clock frequency of .92 Mhz, a low pass (LP) filter, and a Zero Crossing Detector (ZCD). The ZCD is realized by OP-AMP.

Microcontrollers are control-oriented device. Motorola 68HC11 contains A/D converter, input port and output port on the same chip. The data, address, and control buses are implemented on the chip. The supply voltage is stepped down by potential transformer and the output of potential transformer is fed to the ZCD. The ZCD output is fed at the lowest bit of the general purpose input port.

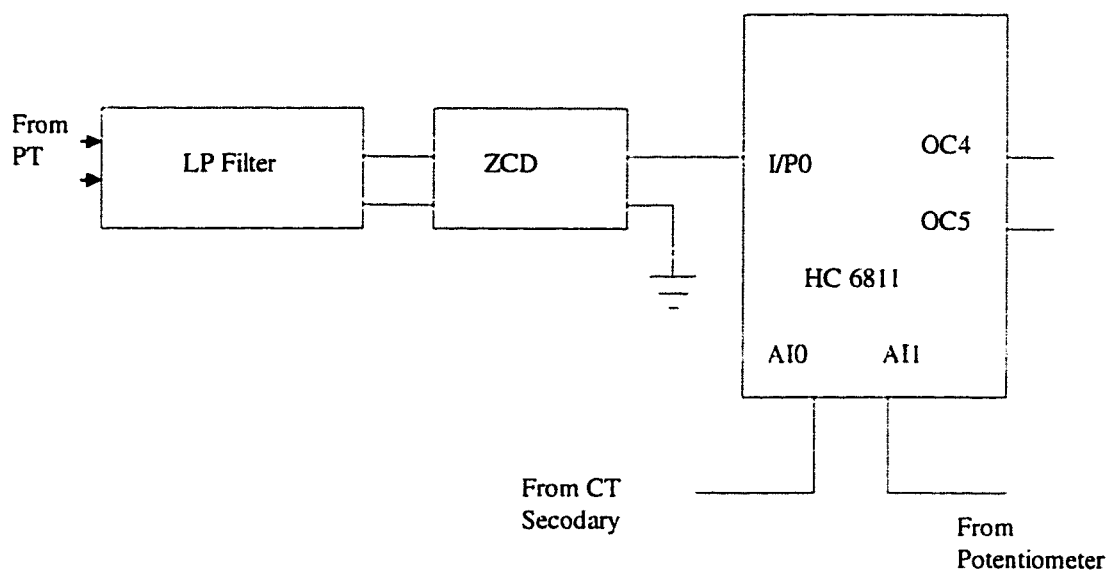


Figure 5.1: Current control block diagram.

The inductor current is sensed by the current transformer and the output of the secondary of the same is fed to one analog input (AI_0) of the microcontroller. The output dc voltage is sensed by the potentiometer, and a known fraction of the dc out put voltage is fed at another analog (AI_1). Finally, the gating signals are taken from the PORTA (OC4 and OC5). Output OC4 drives the gate of MOSFET S_2 and the output of OC5 drives the gate of MOSFET S_1 .

ZCD generates square wave signal, and CPU continuously samples the output of ZCD unless it gets the falling edge or the rising edge of square wave output. Once the falling edge or the rising edge is detected, current control is started. A/D converter of the available microcontroller that has been used in our experiment works from -1 to +1 V and

on reverse logic, as for example it gives 255, 128 and 0 for -1, 0, and 1 respectively. However, it is possible to increase the range by the proper choice of series resistor. Since it works on reverse logic, A/D converter output needs modification. For positive as well as for negative input we need to subtract 128 from the A/D converter output. And then for positive input we need to take 2'S complement after subtraction. After the above modification, the modified digital output varies from 0 to 128 for 0 to ± 1 volt of the analog input.

A low pass filter is placed between the potential transformer output and the input of ZCD to eliminate the harmonics in the supply voltage, and the output of the filter is the fundamental component of supply voltage that is 60Hz. A low pass filter is required, Otherwise ZCD may give false rising and falling edge. Single time constant RC low pass filter has been used which is shown in figure 5.2.

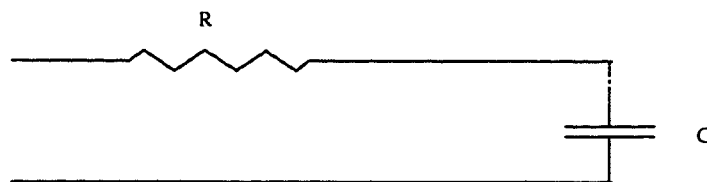


Figure 5.2: Low pass Filter.

The transfer function of this filter is given by

$$H(s) = \frac{1}{1 + \tau s} = \frac{1}{1 + RCs} \quad (5.1)$$

Where $\tau = \frac{1}{2\pi f_0} = \frac{1}{\omega_0}$ and ω_0 is cut-off frequency.

Phase shift between the input and the output of the filter is given by

$$\varphi = \tan^{-1}\left(\frac{X_c}{R}\right) - 90^\circ \quad (5.2)$$

Now f_0 is selected so that fundamental component can pass without attenuation, and at the same it should be well below the third harmonic component, so that later can not appear at output. In our converter circuit we have chosen $f_0 = 90\text{Hz}$, which gives $RC = 1768.38\text{E-}6$. In the selection of R and C, the phase shift has to be taken into consideration. Ideally we want zero phase shift between the input and the output and practically it has to be very close to zero. To ensure nearly zero phase shift we have to satisfy the following condition:

$$X_c \gg R$$

For our circuit we have chosen $R = 10\text{k}$ and $C = 17000\text{pF}$, which gives $X_c = 156\text{K}$ and $X_c/R = 15.6$.

5.2 Interfacing Circuit

The use of isolation transformer at the input side of the converter is usual practice in the industrial applications, because, it prevents the effect of the faults on the dc side or surge from the utilities. It also precludes the use of interface circuit between the power processing block and the control block. However, if isolation transformer is not used interfacing is required. In addition to the interface circuit we need to feed the known

fraction of the output dc voltage to the analog input through isolation amplifier and this isolation amplifier can be realized by the opto-coupler.

Opto-coupler Interfaces between the output of the microcontroller and the gate of the MOSFET. Since source of the two MOSFETs are at same potential therefore, only one dc supply is required for two opto-couplers. Internal structure of opto-coupler is shown in figure 5.3. It consists of a Light Emitting Diode (LED) and a photo transistor. Output of

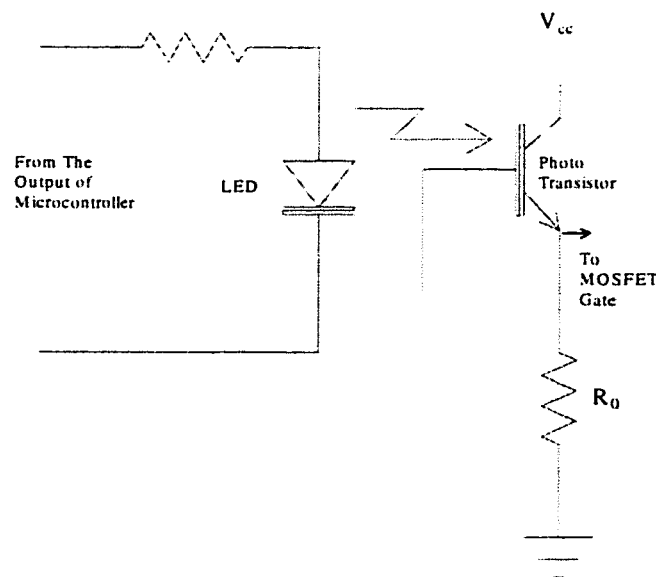


Figure 5.3: Internal structure of Opto-coupler.

the microcontroller output drives the LED. The LED emits infra red light that turns on the photo transistor. The output is taken at the emitter terminal of the transistor and this output is proportional to the input. However, there exist time delay between the input and

output and this time delay depends on output resistor R_0 . Therefore, R_0 should be selected carefully especially at high sampling frequency.

CHAPTER 6

6 CONTROL STRATEGY

The main control objective is to shape the supply current into a sine wave that is in phase with the supply voltage. This results in a unity displacement factor and greatly reduces the supply current harmonics. This is accomplished by operating the switches so as to control the conduction of current over the entire voltage cycle.

6.1 Current Waveshaping

In the unity power factor converter, the supply current is shaped to follow an ideal sinusoidal reference current as closely as possible. The waveshape and phase of the reference current are identical to the supply voltage. The reference current amplitude is controlled by the output voltage control loop to supply the necessary power to the load. In the analog controller, output voltage and supply current are sampled continuously. Depending on the relative magnitude of reference current and actual current, the mode of the control switches is determined. Certain band, called hysteresis band is set, for deciding the mode of the switches, otherwise multistitching problem may arise. In a digital processor based controller, continuous sampling is not possible. The desire to minimize

the amount of processing time spent providing control signals to the converter precludes the use of a strategy that would require the CPU to continuously sample the current. This would be similar to the bang-bang hysteresis control that has been considered by several authors [6], [7].

In the proposed unity power factor converter circuit, we have used the control scheme that is the modified form of the bang-bang hysteresis technique. In this technique supply current is sampled at regular interval and the magnitude of the current is compared with the reference current magnitude at the instant when the supply current is sampled. The state of the switches is decided from the result of comparison. It provides an efficient algorithm that is well suited for implementation using a digital controller such as a microcontroller.

The operation of the current control algorithm is shown graphically in figure 6.1. The reference current is the rectified sinusoidal wave, actual current is sampled at regular interval. The reference position for the sampling the actual current is zero crossing of the supply voltage. A fixed number of sample is taken for each half of the reference current, let us call it sample group. For the purpose of clarity 4 samples/group is assumed. In actual operation sampling frequency is determined by the A/D conversion rate of the microcontroller and the switching losses at power devices. The microcontroller (68HC11) that has been available in the Electrical Engineering laboratory can digitize a sinwave

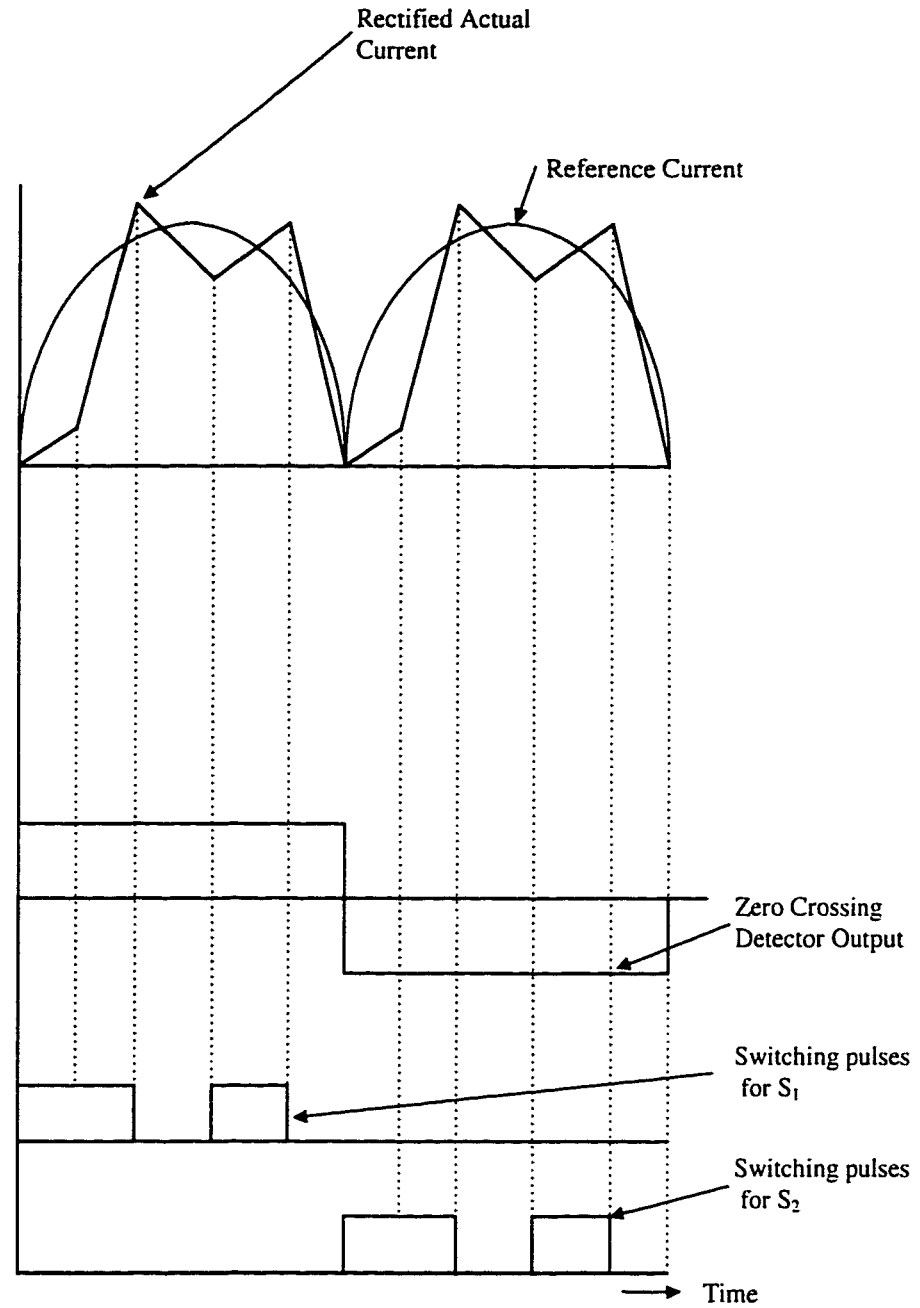


Figure 6.1: Proposed current control strategy.

with frequency upto 10kHz [26]. However, one sample per 104 μ Sec is taken. Therefore, in actual operation 80 samples/group is used. Switches S_1 and S_2 are responsible for

current shaping in positive and negative half respectively. To avoid the unnecessary gating signals switches S_2 and S_1 are kept off in positive and negative cycle respectively. Which switch will take over the charge of controlling the current is decided by the falling and rising edges of the zero crossing detector. When the rising is detected, switch S_2 is turned off until the falling edge is detected. During this time switch S_1 controls the current waveshape. When the falling edge is detected, S_1 is turned off until the rising edge is detected and switch S_2 controls the current during this time.

For the time between the zero crossing and the first sample of a sample group, the relevant switch is kept 'ON'. This eliminates or reduces the dead band. During the regular period, the switching pulses for the power devices are decided from the result of comparison of the sampled current magnitude and the reference current magnitude. If the sampled current magnitude is lower than the reference current magnitude, a pulse of logic '1' is generated. This causes the inductor current to increase in magnitude, as the load and the capacitor are disconnected from the source. Conversely, if the sampled current is higher in magnitude than that of reference current, a pulse of logic '0' is generated, causing inductor current to decrease in magnitude. At this moment the energy stored in the inductor and the energy from the supply source is fed to the capacitor and load.

The current control algorithm, flowchart and software code written in assembly language for the motorola processor are given in appendix B, C, and D respectively.

6.2 Generation of Reference Current

For the generation of reference current, two inputs are needed: one is the amplitude of the reference current and the other one is the Look-Up Table for the instantaneous values for the positive half of a unit amplitude sinusoidal waveform. The former is set initially from the power balance between the input and the output and afterwards it is modulated by the output voltage control loop. The Look Up Table (LUT) for the positive half of unit sinusoidal wave is stored in some specific locations of the control processor. Multiplication of reference current amplitude with the unit sinusoidal signal gives reference waveform, and this is done by the processor.

6.3 Voltage Regulation

Change in the load tends to change the dc bus voltage, therefore closed loop control is required. Regulation of the dc bus voltage is accomplished by varying the amplitude of the reference current wave form.

The input voltage is given by

$$v_{ac} = V_m \sin(2\pi ft) \quad (6.1)$$

If the power conditioning circuit is ideal, the input current will be

$$i_{ac} = I_m \sin(2\pi ft) \quad (6.2)$$

Therefore average input power is

$$P_{in} = \int_0^T v_{ac} i_{ac} dt = \frac{V_m I_m}{2} \quad (6.3)$$

Assuming a resistive load and negligible ripple in the dc bus, the average output power is

$$P_{out} = \frac{V_0^2}{R_L} \quad (6.4)$$

Let V_{ref} is the desired output voltage, then output power is expressed as

$$P_{out} = \frac{V_{ref}^2}{R_L} \quad (6.5)$$

equating the average input power to the output power, we get

$$\frac{V_m I_m}{2} = \frac{V_{ref}^2}{R_L} \quad (6.6)$$

Solving the above equation for I_m gives

$$I_m = \frac{2V_{ref}^2}{V_m R_L} \quad (6.7)$$

An output control loop is used to regulate the dc bus voltage as it varies from the desired voltage. This control adjusts the input reference current amplitude by increasing or decreasing it by an amount proportion to the difference between the actual and the desired values. The dc bus voltage is sampled at rising and falling edge of the zero crossing detector and a new magnitude of the reference current amplitude is calculated, the new current amplitude is

$$I_m(next) = I_m(previous) + K_1(V_{ref} - V_0) \quad (6.8)$$

Sampling of dc bus voltage at the zero crossing of the ac source voltage minimize the influence of 120 Hz ripple in the dc voltage.

CHAPTER 7

7 SIMULATION AND IMPLEMENTATION RESULTS

The proposed converter has been simulated and tested to evaluate the performance. In this chapter simulation and experimental results have been presented.

7.1 Simulation Results

Operation of the power factor correction circuit and model equations for different modes of operation have been presented in chapter 3. Those model equations have been used to simulate the unity power factor converter. MATLAB software has been used for the simulation.

Figure 7.1 represents the ideal sinusoidal reference current and the simulated actual supply current wave. The actual current tracks the reference current. Sampling frequency of 9.6 KHz has been used for the simulation. The sampling frequency is limited by the speed of the microcontroller (68HC11). However, tracking of reference current can be

improved by increasing the sampling rate. Harmonic spectrum of the simulated supply current are shown in figure 7.2a and figure 7.2b for different frequency range.

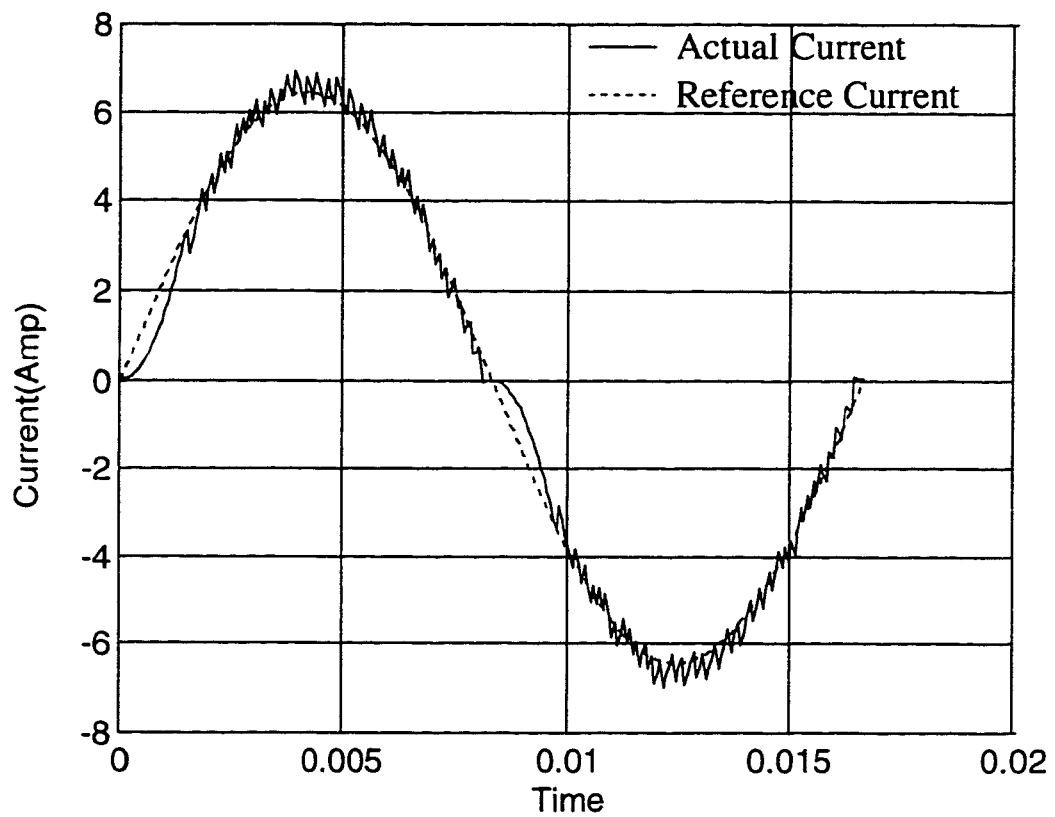


Figure 7.1: Ideal sinusoidal reference current and the simulated actual supply current wave.

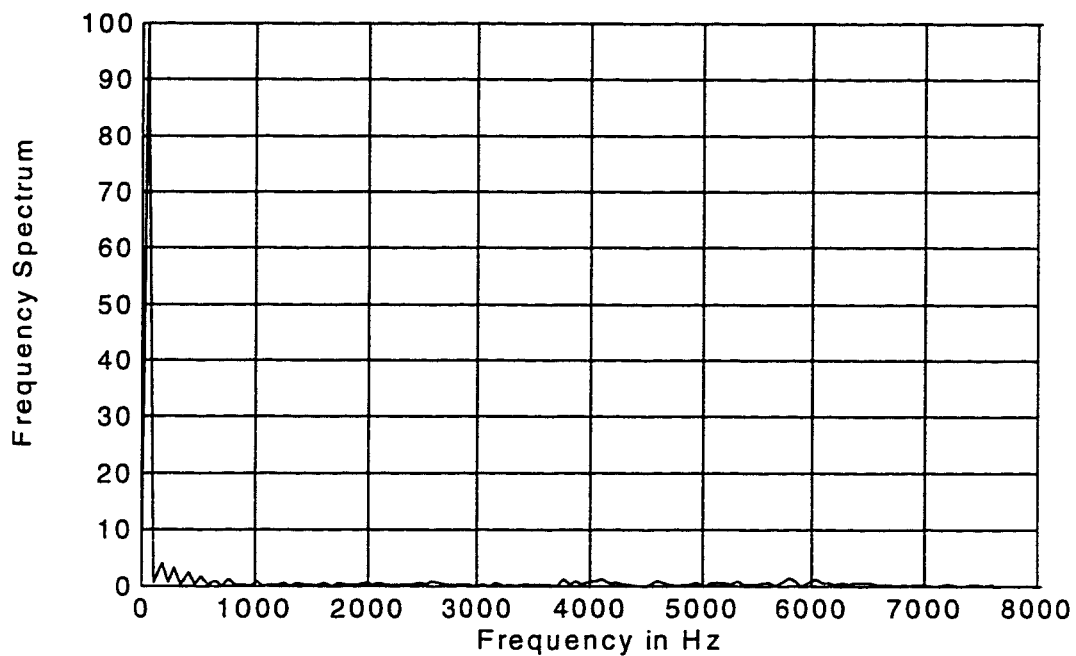


Figure 7.2a: Harmonic spectrum (upto 8 kHz) of the simulated supply current.

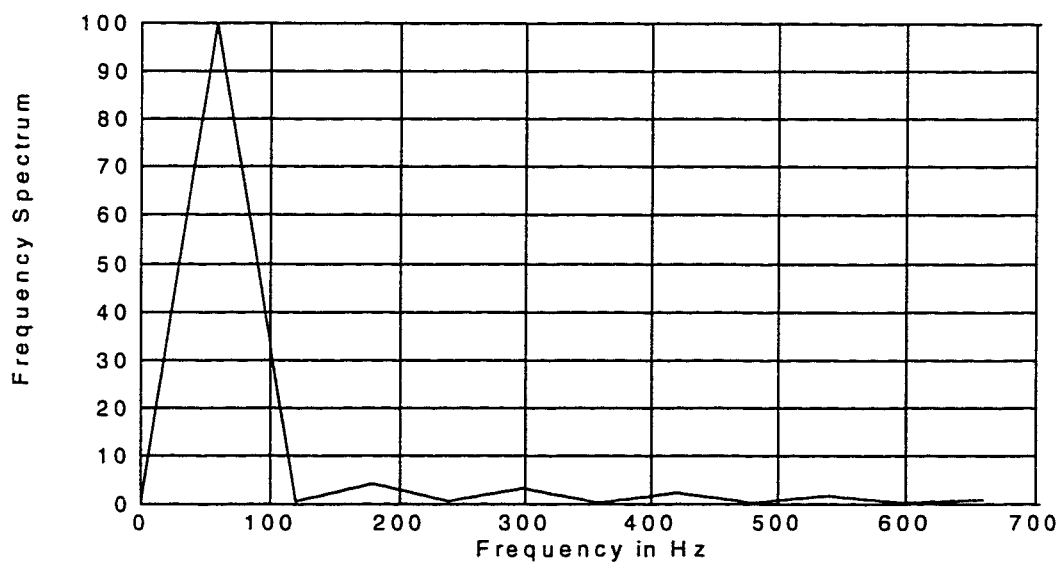


Figure 7.2b: Harmonic spectrum (upto 660 Hz) of the simulated supply current.

7.2 Experimental Set-up

To verify the predicted results an experimental force commutated ac to dc converter has been implemented with the designed value of circuit parameters presented in chapter 4.

The complete power factor correction circuit consists of power processing block and control block. The power processing block is a force commutated ac to dc converter. The control block consists of a microcontroller (68HC11), a low pass (LP) filter, and a zero crossing detector. Signal conditioning circuit such as potential transformer, current transformer, and potentiometer are required to scale down current and voltage. The complete block diagram of the proposed unity power factor converter is shown in Figure 7.3. Different sub blocks, namely LP filter, Zero Crossing Detector, have been described in chapter 5.

The current control algorithm to meet the proposed control strategy and software code written in assembly language for motorola (68HC11) processor have been presented in appendix B and D, respectively. The software code was assembled to generate machine code and finally machine code has been transferred to the user code area of motorola processor from PC by RS 232 interfacing cable.

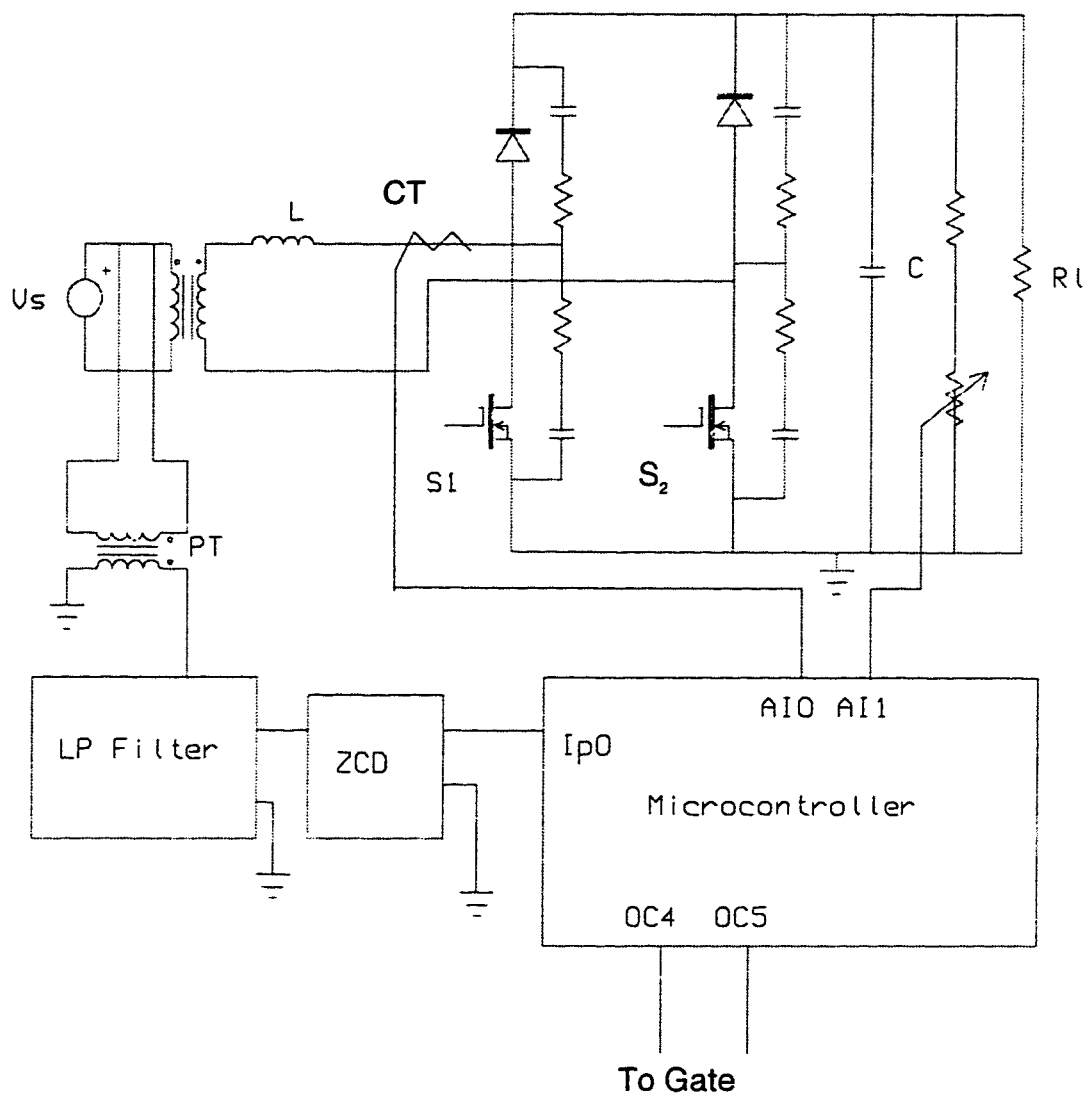


Figure 7.3: Proposed Unity Power Factor Converter.

7.3 Implementation Results

The results obtained from the experiment are presented in this section. The supply current and supply voltage waveform without power factor correction are shown in figure 7.4. The current is of pulsed form and is not in phase of the supply voltage.

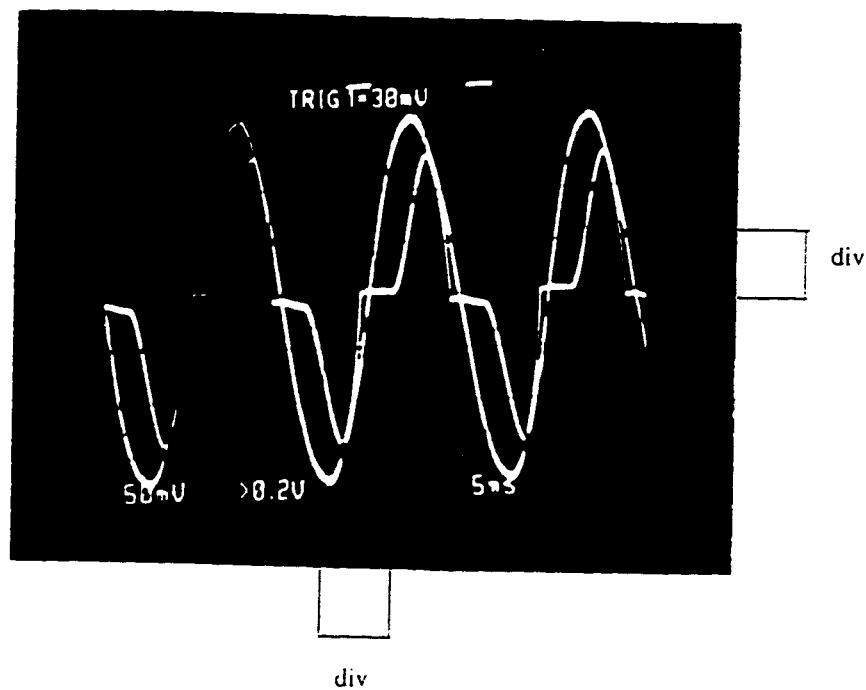


Figure 7.4: Supply voltage (upper trace) and supply current (lower trace) waveform without power factor correction.

Zero crossing detector output is shown in figure 7.5. This is square wave of amplitude 5 volts. Frequency of the ZCD output is equal to the supply frequency, 60 Hz. In the proposed control strategy, The supply current is controlled by different switches in the positive and negative half cycle of the supply voltage. Therefore, it is required to detect the zero crossing of the supply voltage. The falling edge and rising edge of the square wave output from the ZCD represent the negative going and positive going zero crossing of the supply voltage respectively. Therefore, ZCD output decides the control switch in positive and negative half cycles of the supply voltage.

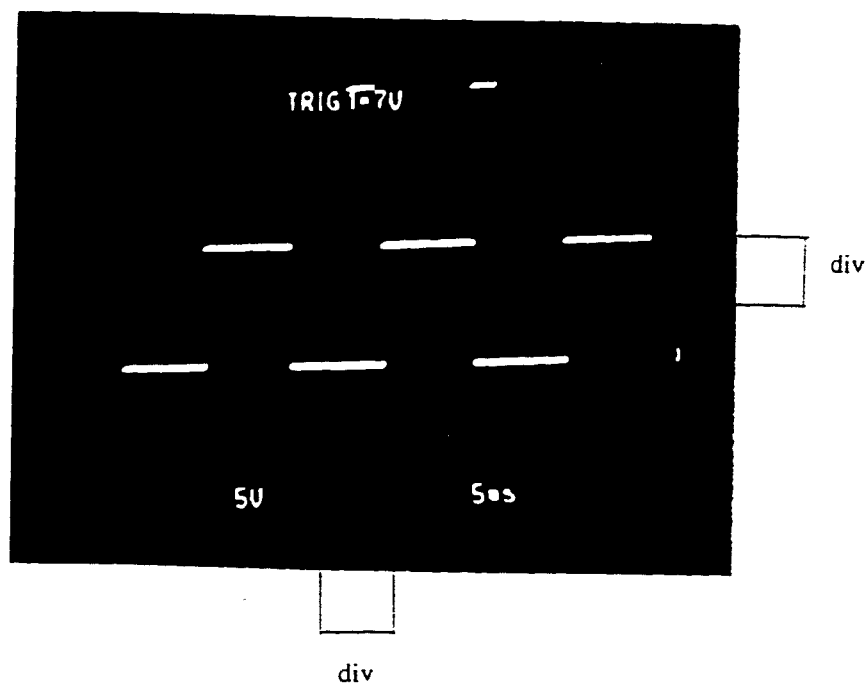


Figure 7.5: Zero crossing detector output.

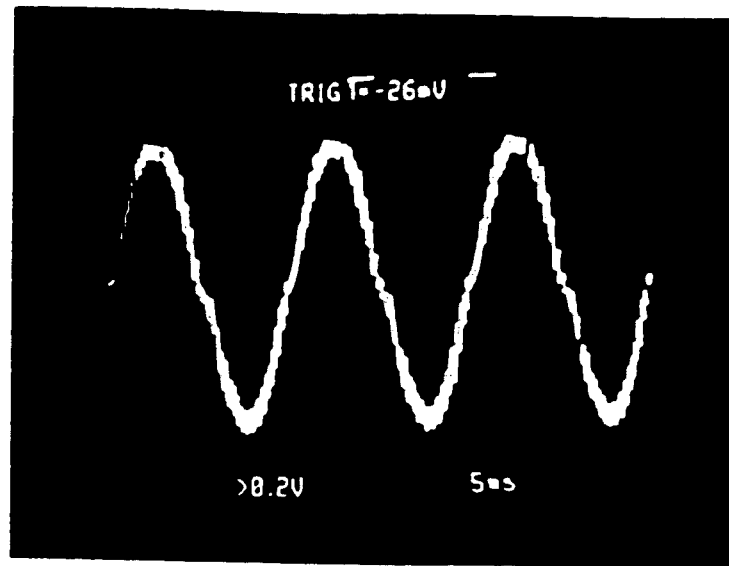


Figure 7.6: Supply current waveform after power factor correction.

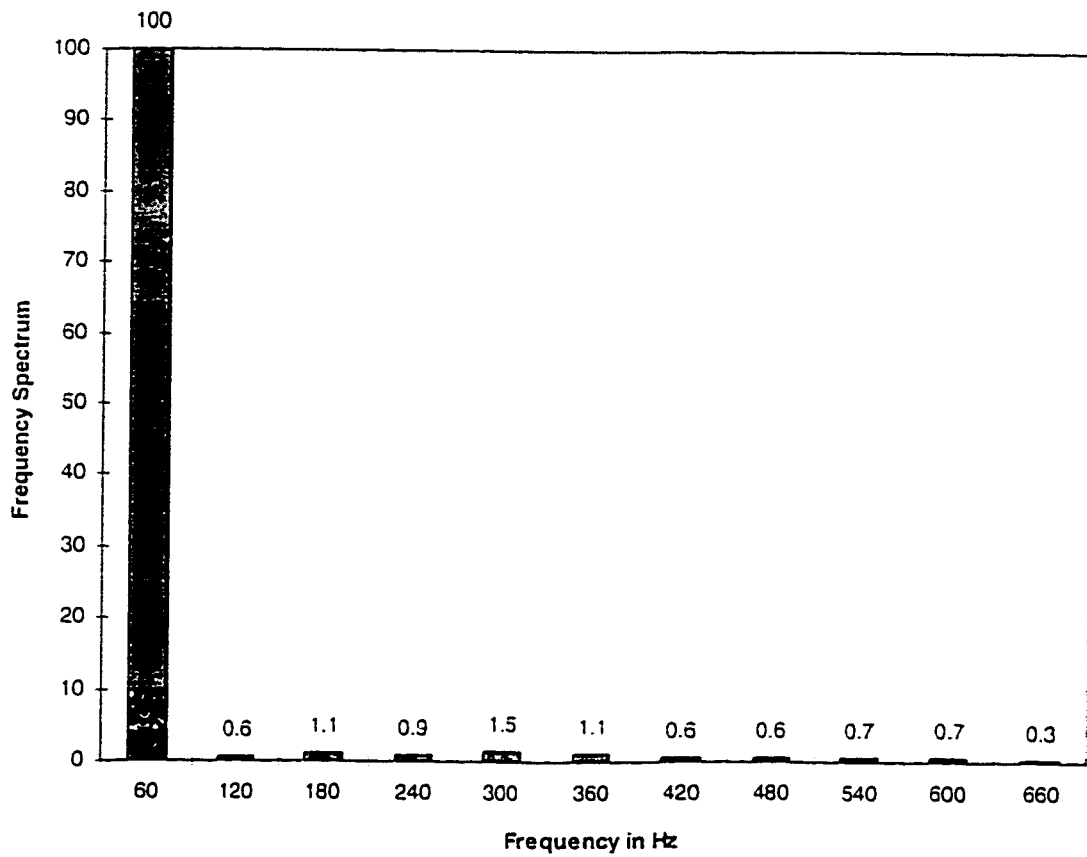


Figure 7.7: Harmonic spectrum of the supply current.

Input current waveform after the power factor correction is shown in figure 7.6, which is almost sinusoidal. Harmonics meter has been used to measure the harmonics and THD of the supply current. Harmonic spectrum of the supply current is shown in figure 7.7. The ratios of the harmonics to the fundamental component are about 1%. Even harmonics in the supply current are due to the slight imbalance of switching in positive and negative half. An average THD of 4.88% has been recorded. The experimental waveform of supply voltage and supply current after the power factor correction are shown together in figure 7.8. From the figure it is obvious that supply current is synchronised with the supply voltage.

The supply current waveform and its harmonic spectrum obtained from the laboratory implementation are consistent with those obtained from the simulation.

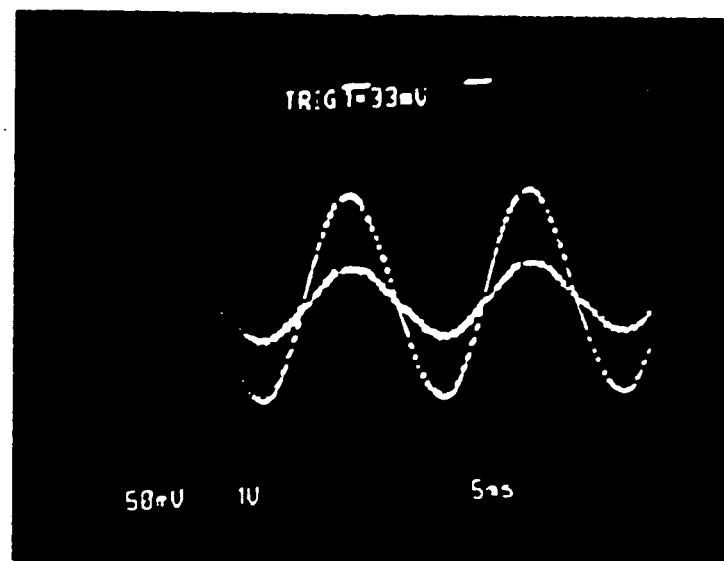


Figure 7.8: Supply voltage (upper trace) and supply current (lower trace) waveform after power factor correction.

The capacitor voltage (figure 7.9) contains the ripple component, which fluctuates with twice the supply frequency as in the conventional bridge connection of diode. The RMS Ripple factor of that voltage is 1.41%.

Pulse width modulated output at port OC4 of the microcontroller is shown in figure 7.10. Pulse width output at port OC5 is 180° out of phase of that at port OC4. These pulse width modulated outputs drive the MOSFET gates.

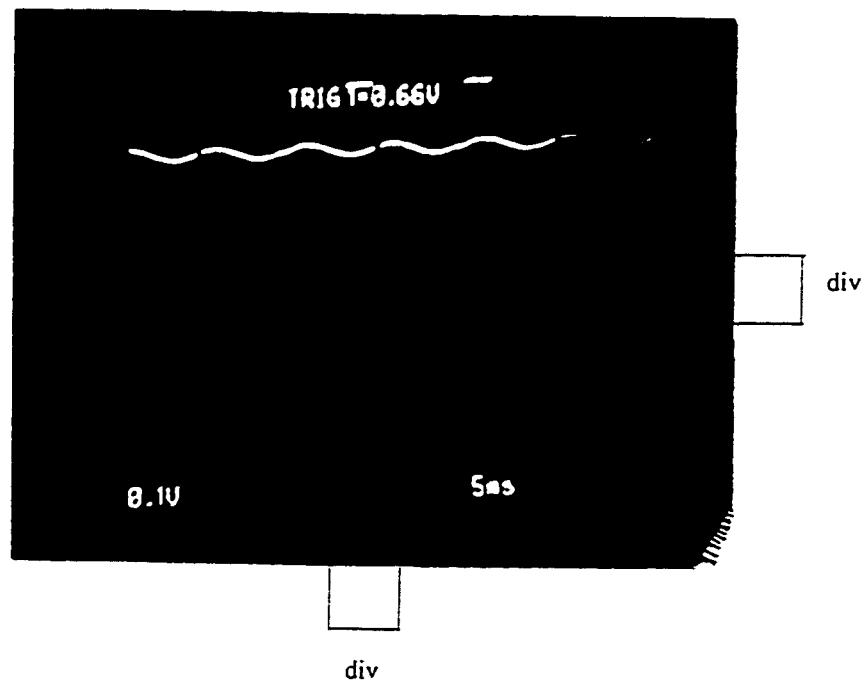


Figure 7.9: Output dc voltage.

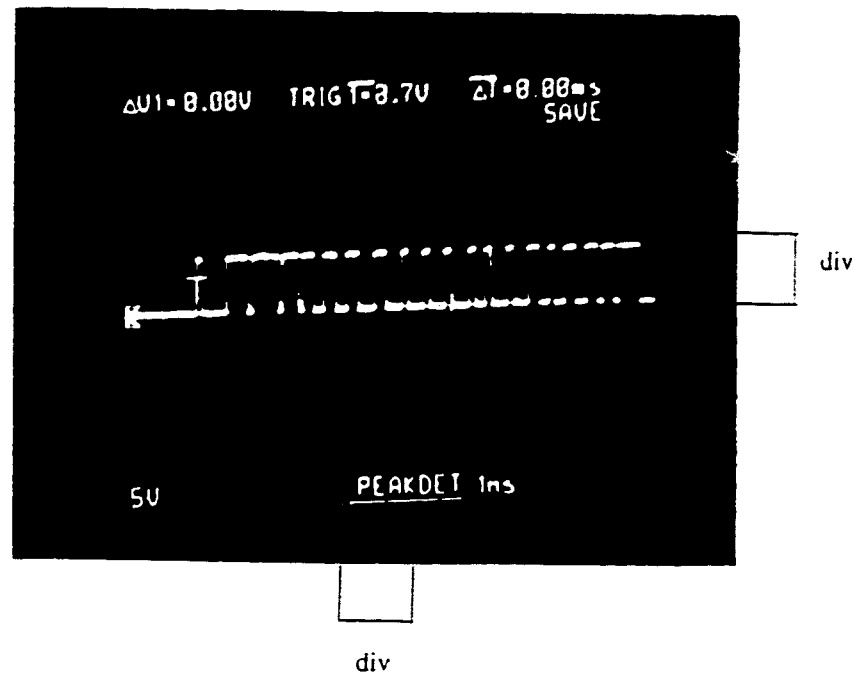


Figure 7.10: Pulse-width modulated output from microcontroller.

7.4 Comparisons

The main objective of the research was to replace the discrete blocks in control circuitry presented [6]-[11] by microcontroller without sacrificing the performance. The performance of the proposed unity power factor converter is promising and it satisfies the IEC-555-2 harmonic requirement. Performance parameter, such as THD, power factor of the converters presented in [6]-[9] have not been reported. Although supply current of all

the converter [6]-[11] are nearly sinusoidal and are in phase of the supply voltage, the proposed unity power factor converter has the following advantages:

- Satisfactory performance with simple control circuitry
- It has the advantage over the analog ones, because the control strategy and configuration can be modified at the software level providing a high operation and adaptation flexibility.
- It also gives reduced parts count and enhanced reliability.
- For high frequency power electronic converter and for complicated control scheme analog technique is inadequate.

CHAPTER 8

8 CONCLUSIONS AND SUGGESTION

This chapter presents the conclusions arising from the results described in the previous chapter and gives suggestions for the further research work.

8.1 Conclusions

A microcontroller based unity power factor converter has been proposed. The most important feature of the proposed converter is its satisfactory performance with simple control circuitry. Hardware that has been used in the proposed converter is the minimum for the microcontroller based unity power factor converter. The zero crossing detector does the synchronization job.

The operation of the resulting converter circuit has been described in details. Complete design equations for power processing circuit and the device and components' ratings have been provided.

In the proposed converter circuit, the educational version 68HC11 motorola microcontroller has been used, the speed of which is 0.92 Mhz and the A/D converter of the same takes 128 clock cycle for each conversion. Therefore, speed of the

microcontroller limits the highest possible sampling frequency. For our experiment sampling frequency of 9.6 KHz has been used. The use of microcontroller with higher speed such as 87C51Ga with speed 12 Mhz or 68HC16 with speed 16.8Mhz will increase the performance, make the converter more compact and noiseless.

8.2 Suggestion for Further Research Work

The proposed control strategy has been tested for single phase ac to dc converter. Now the work may be extended to three phase system.

Appendix A Simulation Program in MATLAB

```
% simulation of the proposed unity power factor converter
clear all;
tstep=0.1041625*10^(-3);
C=10765.4/377.14 ;
actsig=- 10765.4/377.14 *cos(377.14*tstep) + C;%f1(tstep);
actsigv=[0,actsig];
refsigv=[0];

for t= 2*tstep:tstep:8.334*10^(-3)
    refsig=6.428*sin(2*pi*60*(t-tstep));refsigv=[refsigv,refsig];
    if refsig >= actsig
        C=actsig + 10765.4/377.14 *cos(377.14*(t-tstep)) ;
        actsig1=- 10765.4/377.14 *cos(377.14*t) + C ;
        actsig=actsig1;actsigv=[actsigv,actsig];
    else
        C=actsig + 10765.4/377.14 *cos(377.14*(t-tstep)) + 15224.91*(t-tstep);
        actsig2=- 10765.4/377.14 *cos(377.14*t) - 15224.91*t + C;
        actsig=actsig2;actsigv=[actsigv,actsig];
    end;
end;
refsigv=[refsigv,0];
C= -10765.4/377.14 ;
actsig=- 10765.4/377.14 *cos(377.14*(8.334*10^(-3)+tstep)) + C;
actsigv=[actsigv,actsig];
```

```

for t= (8.334*10-3)+2*tstep:tstep:16.668*10-3)
refsig=6.428*sin(2*pi*60*(t-tstep));refsigv=[refsigv,refsig];
if abs(refsig) >= abs(actsig)
C=actsig + 10765.4/377.14 *cos(377.14*(t-tstep)) ;
actsig3=- 10765.4/377.14 *cos(377.14*t) + C ;
actsig=actsig3;actsigv=[actsigv,actsig];
else
C=actsig + 10765.4/377.14 *cos(377.14*(t-tstep)) - 15224.91*(t-tstep);
actsig4=- 10765.4/377.14 *cos(377.14*t) + 15224.91*t + C;
actsig=actsig4;actsigv=[actsigv,actsig];
end;
end;
refsigv=[refsigv,0];
supsigv=[0]
for t= tstep:tstep:16.668*10-3)
supsig= 15.556*sin(2*pi*60*t);
supsigv=[supsigv, supsig];
end;
t=0:tstep:16.668*10-3);
figure(1);plot(t,actsigv,'-r',t,refsigv,'*b');
grid;
xlabel('Time');
ylabel('Current(Amp)');
legend('Actual current', 'Reference current');
figure(2);plot(t,supsigv,'*b',t,actsigv,'-r');
grid;
xlabel('Time');
legend('Supply voltage', 'Supply current');
tstep=0.1041625*10-3);

```

```

fsam=1/tstep;
freq = fsam/256*(0:127);
y=fft(actsigv);
N=length(actsigv);
f=fsam*(0:N-1)/N;
figure(3);plot(f(1:80),abs(y(1:80)),'r');
grid;
xlabel('Frequency in Hz');
ylabel('Frequency Spectrum');
a=lpc(actsigv,40);
om=-pi:0.01:pi;
Xact=freqz(1,a,om);
lx=length(om);
figure(4);plot(fsam*om(lx/2+1:lx),abs(Xact(lx/2+1:lx)),'r');
grid;
xlabel('Frequency in Hz');
ylabel('Frequency Spectrum');

```

Appendix B Current Control Algorithm

Sample values of only Positive half of the unit sinusoidal wave are stored in some specific location of control processor memory. Output Voltage (V_0) is sampled at twice the line frequency. In positive half S_2 is always off and in negative half S_1 is always off.

Step 1 : Set $I_m = I_{mi}$

Turn off S_1 and S_2

Step 2 : Read output of ZCD

If ZCD = 0 GO TO Step 3

If ZCD = 1 GO TO Step 4

Step 3 : Read Output of ZCD

If ZCD = 0 Continue to sample output of ZCD

If ZCD = 1 Turn on S_1 and Turn off S_2 and GO TO Step 5

Step 4 : Read Output of ZCD

If ZCD = 1 Continue to sample the output of ZCD

If ZCD = 0 Turn on S_2 and Turn off S_1 and GO TO Step 9

- Step 5 : Read output voltage V_0
 Compute $U = (V_{ref} - V_0)$
 Compute $I_m = I_m (\text{previous}) + KU$
 Load Starting Address (TABS) of Look-Up Table (LUT) to Counter X
- Step 6 : Compute $|I_r| = I_m * \text{Content of Location Pointed by Counter (X)}$
 Read I_L and Compute $\Delta = |I_r| - |I_L|$
- Step 7 : Check whether $\Delta \geq 0$
 If YES Turn on Switch S_1
 ELSE Turn off Switch S_1
- Step 8 : Increment the counter by 1
 Compare the counter content (X) with the ending address (TABE) of LUT
 If $X > \text{TABE}$ Turn on S_1 and GO TO Step 4
 ELSE Go To Step 6
- Step 9 : Read output voltage V_0
 Compute $U = (V_{ref} - V_0)$
 Compute $I_m = I_m (\text{previous}) + KU$
 Load Starting Address (TABS) of Look-Up Table (LUT) to Counter X

Step 10 : Compute $|I_r| = I_m * \text{Content of Location Pointed by Counter (X)}$

Read I_L and Compute $\Delta = |I_r| - |I_L|$

Step 11: Check whether $\Delta \geq 0$

If YES Turn on Switch S_2

ELSE Turn off Switch S_2

Step 12 : Increment the counter by 1

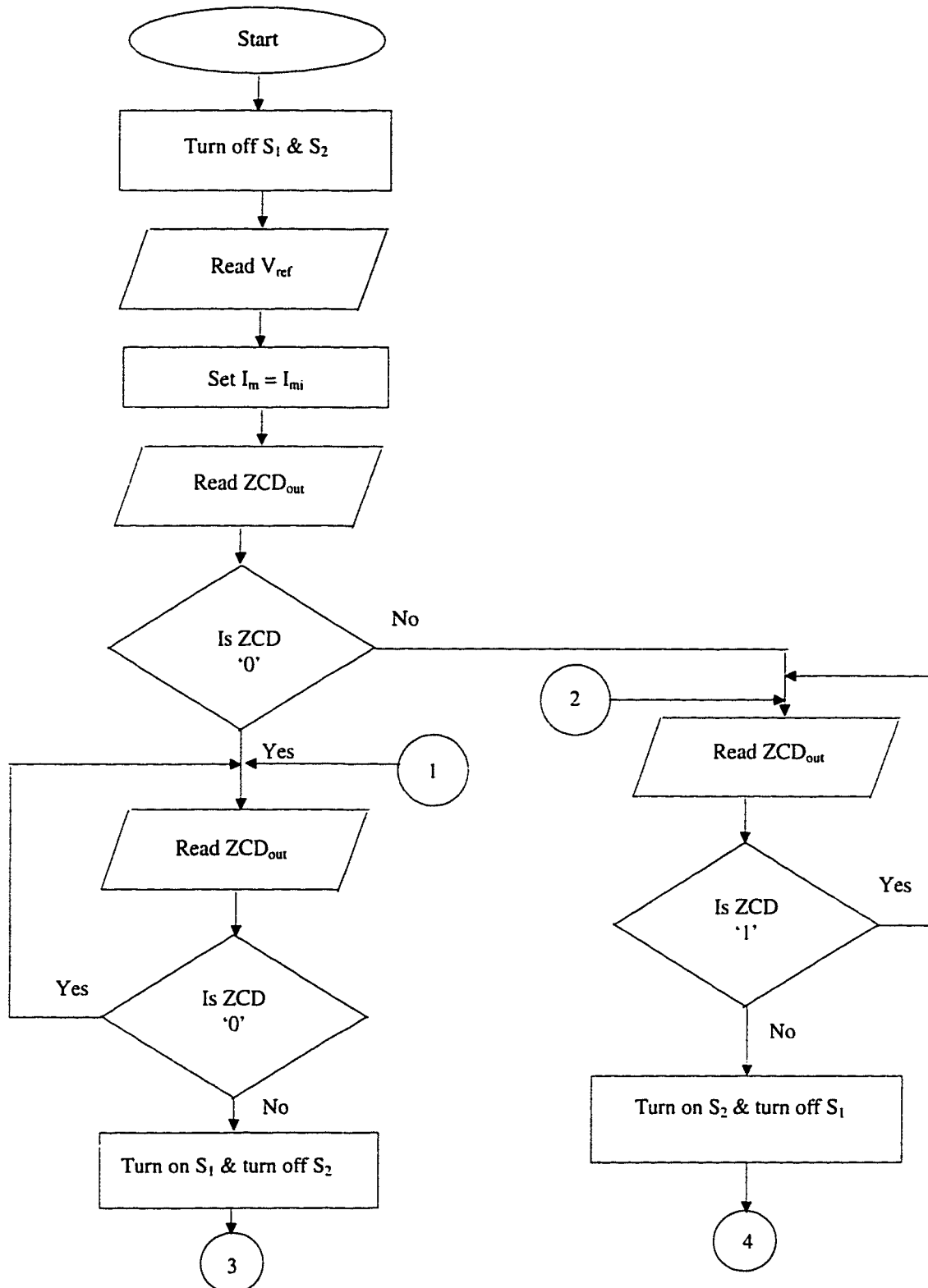
Compare the counter content (X) with the ending address of LUT

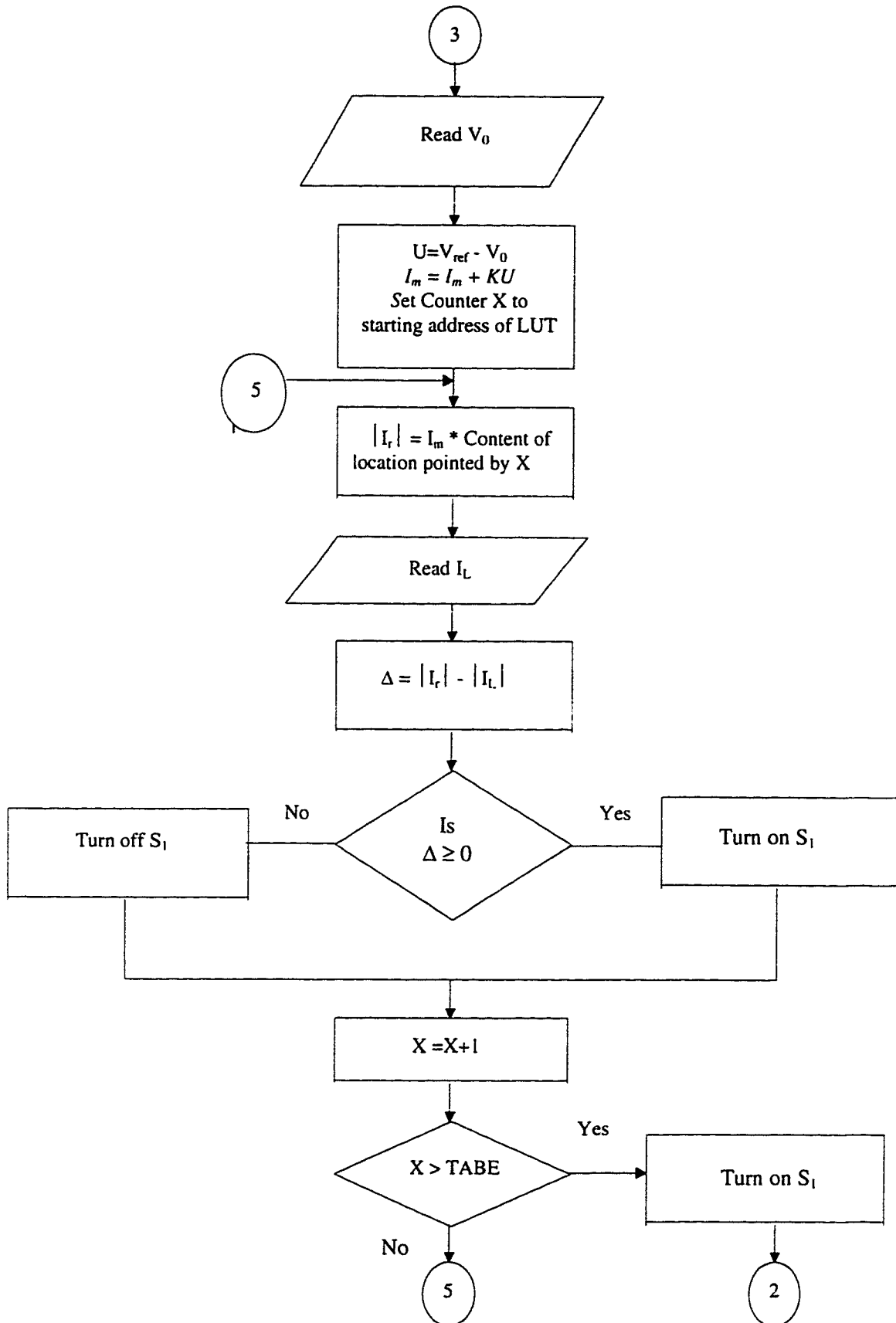
(TABE)

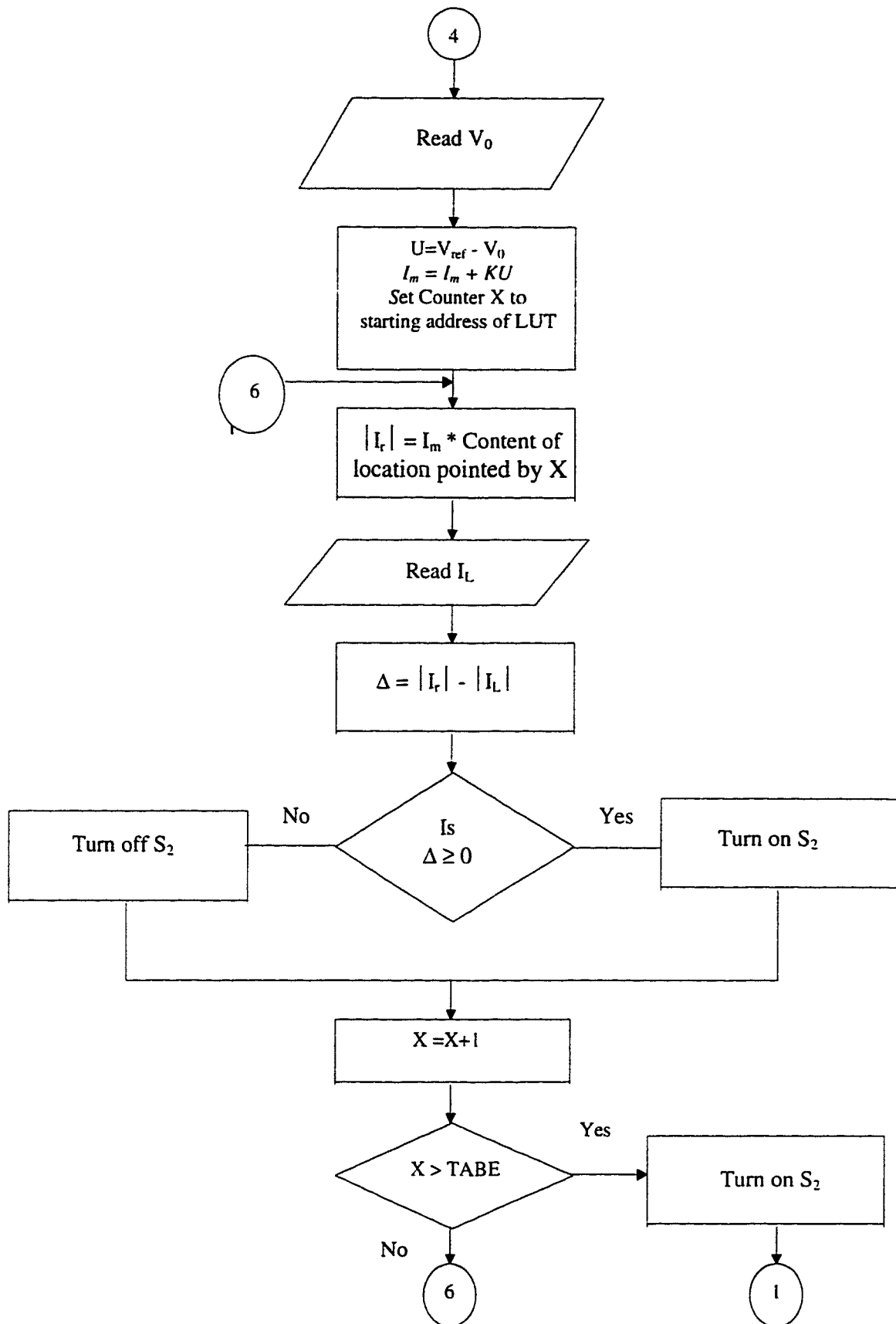
If $X > \text{TABE}$ Turn on S_2 and GO TO Step 3

ELSE Go To Step 10

Appendix C Current Control Flow Chart







Appendix D Software Code In Assembly Language for Motorola Processor

* PROGRAM WRITTEN IN ASSEMBLY LANGUAGE

* FOR THE 6811 MOTOROLA PROCESSOR

* SAMPLE PERIOD IS 104 USEC

*INITIALIZATION BLOCK

```
IP_PT EQU  $B280    ; Address of the input port
ADCTL EQU  $B030    ; Address of the a/d control resistor
ADR1  EQU  $B031    ; Address of the data resistor
PORTA EQU  $B000    ; Address of the porta
ST_PTR EQU  $3000    ; Highest address of the stack
CMAX  EQU  $F0      ; address of the loc.for storing ref. current
TABS  EQU  $1001    ; starting address of the lut
TABE  EQU  $1050    ; ending address of the lut
VREF  EQU  $30      ; scaled ref.voltage
```

* MAIN PROGRAM

```
ORG  $0000    ; starting address of the code
```

```

LDS    #ST_PTR

JMP    GETHBYT    ; ask for the initial reference amplitude

STAB    CMAX

CLR    PORTA    ; reset the PORTA

START   LDAA    IP_PT

        LSRA                ; check the LSB of IP_PT

        BCC    RISEG

FALEG   LDAA    IP_PT    ; Looking for the falling edge

        LSRA

        BCS    FALEG

        LDAB    #$10    ; Turn on the switch s2

        STAB    PORTA

        JSR    IMAX

READN   LDAB    #00

        STAB    ADCTL    ; Make the request for a/d conversion

        LDAB    0,X    ; Load the con.of the loc.pointed by counter x

        LDAA    CMAX

        MUL

        ADCA    #$00    ; Acc.A has the instan. Value of ref. Current

        NOP

        NOP

```

```

NOP
NOP
LDAB  ADR1      ; get the a/d conversion result
SUBB  #$80
TSTB
BGE   NOTS1
COMB
INCB
NOTS1 SBA
      BHS  SWONN
      LDAB #00
      BRA  OPLODN
SWONN LDAB  #$10
OPLODN STAB  PORTA
      INX
      CPX  #TABE
      BLS  DELAYN
      LDAB #$10
      STAB PORTA
      JMP  RISEG
DELAYN LDAB  #03

```

```
WAITN    DECB

          CMPB  #00

          BNE   WAITN

          BRA   READN

RISEG    LDAA  IP_PT

          LSRA

          BCC   RISEG

          LDAB  #$08

          STAB  PORTA

          JSR   IMAX

READP    LDAB  #00

          STAB  ADCTL

          LDAB  0,X

          LDAA  CMAX

          MUL

          ADCA  #$00

          NOP

          NOP

          LDAB  ADR1

          SUBB  #$80

          TSTB
```



```

        BGE  NOTS2
        COMB
        INCB
NOTS2   SBA
        BHS  SWONP
        LDAB #00
        BRA  OPLODP
SWONP   LDAB #$08
OPLODP  STAB PORTA
        INX
        CPX  #TABE
        BLS  DELAYP
        LDAB #$08
        STAB PORTA
        JMP  FALEG
DELAYP  LDAB #03
WAITP   DECB
        CMPB #00
        BNE  WAITP
        BRA  READP
```

IMAX

LDAB #01

STAB ADCTL

LDAA #VREF

LDAB #08

WAIT

DECB

CMPB #00

BNE WAIT

LDAB ADR1

SUBB #\$80

COMB

INCB

CMPB #VREF-10

BLO GAHED

CMPB #VREF+10

BHI GAHED

SBA

ASRA

ADDA CMAX

STAA CMAX

GAHED

LDX #TABS

RTS

* DATA SECTION

ORG TABS

FCB 10,20,30,40,50,60,70,79,89,98,107,116,125,134,142

FCB 150,158,166,174,181,188,195,201,207,213,218,223

FCB 228,232,236,240,243,246,249,251,253,254,255,255

FCB 255,255,255,254,253,251,249,247,244,240,237,233,228

FCB 224,219,213,207,202,195,189,182,175,167,159,151,143

FCB 135,126,117,108,99,90,80,71,61,51,41,31,22,11,2

END

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